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Review paper on design and implementation of FFT processor using memory based pipelined architecture

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Abstract
The Fast Fourier Transform (FFT) is an efficient algorithm for computing the Discrete Fourier Transform (DFT) and requires less number of computations than that of direct evaluation of DFT. It has several applications in signal processing. Because of the complexity of the processing algorithm of FFT, recently various FFT algorithms have been proposed to meet real-time processing requirements and to reduce hardware complexity over the last decades. This work presents combined pipelined architecture with memory based architecture to get an area and time efficient architecture that could be used as a coprocessor with built in all resources necessary for an embedded DSP application.
The design simulation and its FPGA based implementation have to be verified using Xilinx ISE 14.1 tool using VHDL.

Keywords: Radix, FFT, Xilinx, Memory

1. Introduction
Fast Fourier Transform (FFT) processing is an important aspect of many Digital Signal Processing applications and systems. Real-time or fast execution is an important criteria for many applications. For example, wide-band Orthogonal Frequency Division Modulation (OFDM) systems, biomedical instrumentation and radar usage in military domain are some of the applications requiring high-speed and large-point FFT systems as one of their key components. FFT architectures with structured pipelines have been commonly used to meet the fast, real-time processing demands. But pipeline FFT processors suffer the problem of being memory-bandwidth limited for large-point FFTs. The FFT is a common digital signal processing function used across a multitude of application domains. Modern communication systems such as Orthogonal Frequency Division Multiplexing (OFDM) rely on the high speed computation of the FFT. Radar systems also employ the FFT for matched filtering and Doppler processing [1]. The FFT algorithm should be chosen here to consider the execution speed, hardware complexity, and flexibility and precision [2]
FFT is used to speed up the DFT, it reduces the computation time required to compute a discrete Fourier transform and improves the performance by factor 100 or more over direct evaluation of DFT. The SDF pipelined architecture is used for the high-throughput in FFT processor. There are three types of pipeline structures; they are single-path delay feedback (SDF), single-path delay commutator (SDC) and multi-path delay commutator. The advantages of single-path delay feedback (SDF) are (1) This SDF architecture is very simple to implement the different length FFT. (2) The required registers in SDF architecture is less than MDC and SDC architectures. (3) The control unit of SDF architecture is easier [3].

2. Literature review
SDF FFT architectures make use of delay-lines implemented using memory and shift registers to reorder data at each butterfly stage. Delay-lines of length 2_ are required for all _ from 0 to log__ − 1 where is the number of FFT points the SDF FFT processor is capable of computing. This requirement is due to the data shuffling intrinsic to the decimate-in-time (DIT) and decimate-in-frequency (DIF) algorithms and so called Parallel Extensions to Single-Path Delay-Feedback FFT Architectures [1]

The Fast Fourier transform (FFT) and Inverse Fast Fourier Transform (IFFT) processing is one of the key procedures in popular orthogonal frequency division multiplexing (OFDM) communication systems. Structured pipeline architectures, low power consumption, high speed and reduced chip area are the main concerns in this VLSI implementation the optimization of space between two slots is the main part of this research work. [2]

The FFT algorithm should be chosen here to consider the execution speed, hardware complexity, and flexibility and precision. There different types of methods and algorithms of FFT [3]

The Discrete Fourier transform (DFT) is one of the fundamental operations in the field of digital signal processing. The DFT, with a transform length equal to a power of 2, is usually implemented with the fast Fourier transform (FFT). In many applications, such as asymmetric digital subscriber [4]

Fast Fourier Transform (FFT) algorithm intensive computational requirements, it occupies large area and consumes high power if implemented in hardware. Efficient algorithms are developed to improve its architecture. In this paper, a variety of available FFT algorithms are presented and then different architectures are outlined by exploring the techniques and algorithms involved in each of the architectures. The widely adopted architectures and trends in architectural modification to reduce power consumption and area and to achieve high throughput are discussed. Also the memory based architectures are classified into single memory architecture and dual memory architecture. In single memory architecture, the processing element is connected to a single memory unit of at least N words by a bidirectional bus as shown in fig. 1.

Fig 1: Single Memory Architecture

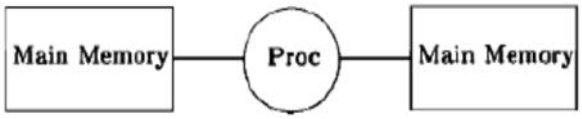


Fig 2: Dual memory Architecture

The different architectures such as Cache memory, the delay and feedback systems The trends in architectural optimization and various modifications to baseline architectures proposed in the literature are reviewed and the algorithms adopted for the state of the art architectures are available [5]

In the paper [1] it has proposed a set of extensions that can be used to apply parallelism to the Radix-22 SDF FFT pipeline. The proposed methods are flexible and allow for 8 -point

FFT and IFFT computation such that is a power of two. Additionally, both the DIF and the DIT algorithms are supported. Although the stated extensions apply specifically to the Radix-22 SDF algorithm, similar techniques could be used for all pipelined SDF FFT implementations. The proposed extensions impose no restrictions on the overall throughput of the FFT circuit given adequate resource availability. Synthesis experiments were conducted to analyze how parallelization of the pipeline affects the size, throughput and power of the circuit. It was determined that there are significant benefits in terms of both area efficiency and energy efficiency when increasing the parallelism of the FFT. These benefits can be attributed to the fact that the memory requirements of the delay-lines remain approximately constant regardless of the parallelization factor.

FFT processor architecture optimized for speed of computation and area reduction has been designed. The algorithm used was a modified version of the DIF-FFT with the inputs and the outputs in natural order (not in bit reversed order). This design eliminates the need of scrambling the inputs and outputs. Although the processor designed is quite small and fast there are some improvements that can be made. Most of the cells used to build the FFT processor have been optimized for speed, area and power consumption. Implementing this technique of taking complex conjugate from some of the outputs recommended for higher point FFTs. The power consumption can be reduced up to 70% [2].

As, it has been shown the application of FFT is that mathematical analysis of signals. To make it flexible for N point and implement it on real time hardware. In this we will use the parallel multiplier will give output in one clock cycle independent of the number of bits at the input in normal cases form bit multiplier it requires n clock cycle which makes it slow so, for 16 bit clock cycle while in or case output will come in one clock cycle [3].

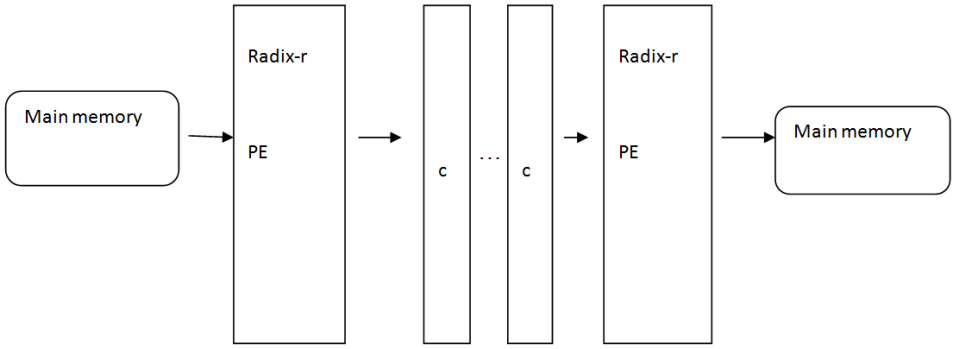
Long-length -point FFT's that are required by many DSP systems, such as ADSL and OFDM. The previous VLSI architectures for FFT implementation have long latency of and relatively low throughput rate. The FFT architectures in this brief can improve the previous FFT designs by reducing the latency by a factor of 2 and by increasing the throughput rate by a factor of two. The author proposed FFT architectures are very suitable for long-length high-speed FFT applications [4]

Basic architectures for FFT implementations are explored and a comparison between the widely adopted architectures in terms of hardware complexity and scope of optimization is discussed. The trends in architectural optimization and various modifications to baseline architectures proposed in the literature are reviewed and the algorithms adopted for the state of the art architectures [5]

3. Proposed Work

Memory based architecture is used for radix-r N point FFT implementation. Memory based is good when complexity of hardware is main concern and pipeline architecture is good when performance and power are main concern.

Our new approach is to design and implement radix-2 8 point FFT by combined memory based pipelined architecture the proposed -FFT processor will requires fewer computation cycles and lower cost compared to prior work. Maintained a lower hardware complexity. It is very suitable for applications in implantable or portable devices because of its low area and power consumption.



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