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Simulation of low power 9 Tfull adder with reduced ground bounce noise technology

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Abstract
Low power has emerged as a principal theme in today's world of electronics industries. Power dissipation has become an important consideration as performance and area for VLSI Chip design. With shrinking technology reducing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. For power management leakage current also plays an important role in low power VLSI designs. Leakage current is becoming an increasingly important fraction of the total power dissipation of integrated circuits.
An adder is one of the most critical components of a processor which determines its throughput, as it is used in the ALU, the floating-point unit, and for address generation in case of cache or memory access. Recently there have been several attempts to design energy recovering logic in the pursuit of energy efficient circuitry. In this paper we are going to design aultra low power 14 Transistor adder using the novel stacking power gating logic which has very low leakage power.

Keywords: Simulation; Low Power 9 TFull Adder; Ground Bounce Noise Technology

1. Introduction to VLSI

Digital systems are highly complex at their most detailed level. They may consist of millions of elements i.e., transistors or logic gates. For many decades, logic schematics served as then guafranca of logic design, but not anymore. Today, hardware complexity has grown to such a degree that a schematic with logic gates is almost useless as it shows only a web of connectivity and not functionality of design. Since the 1970s, computer engineers, electrical engineers and electronics engineers have moved toward Hardware description language (HDLs).

Digital circuit has rapidly evolved over the last twenty five years .The earliest digital circuits were designed with vacuum tubes and transistors. Integrated circuits were then invented where logic gates were placed on a single chip. The first IC chip was small scale integration (SSI) chips where the gate count is small. When technology became sophisticated, designers were able to place circuits with hundreds of gates on a chip. These chips were called MSI chips with advent of LSI; designers could put thousands of gates on a single chip. At this point, design process is getting complicated and designers felt the need to automate these processes.

With the advent of VLSI technology, designers could design single chip with more than hundred thousand gates. Because of the complexity of these circuits computer aided techniques became critical for verification and for designing these digital circuits.

One way to lead with increasing complexity of electronic systems and the increasing time to market is to design at high levels of abstraction. Traditional paper and pencil and capture and simulate methods have largely given way to the described UN synthesized approach.

For these reasons, hardware description languages have played an important role in describe and synthesis design methodology. They are used for specification, simulation and synthesis of an electronic system. This helps to reduce the complexity in designing and products are made to be available in market quickly. The components of a digital system can be classified as being specific to an application or as being standard circuits. Standard components are taken from a set that has been used in other systems. MSI components are standard circuits

and their use results in a significant reduction in the total cost as compared to the cost of using SSI Circuits. In contrasts, specific components are particular to the system being implemented and are not commonly found among the standard components.

The implementation of specific circuits with LSI chips can be done by means of IC that can be programmed to provide the required logic.

2. 9T Full Adder

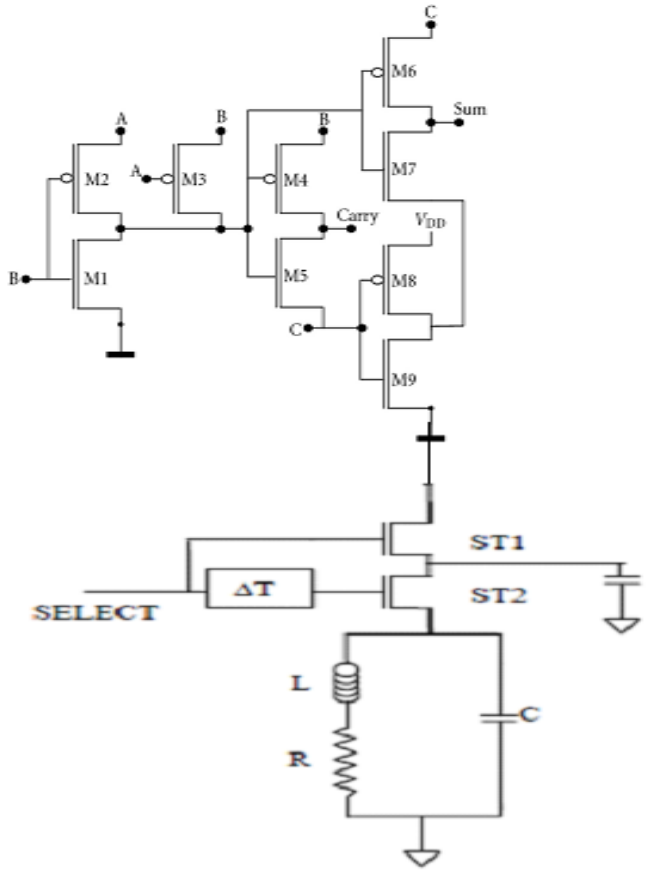

Fig: 1

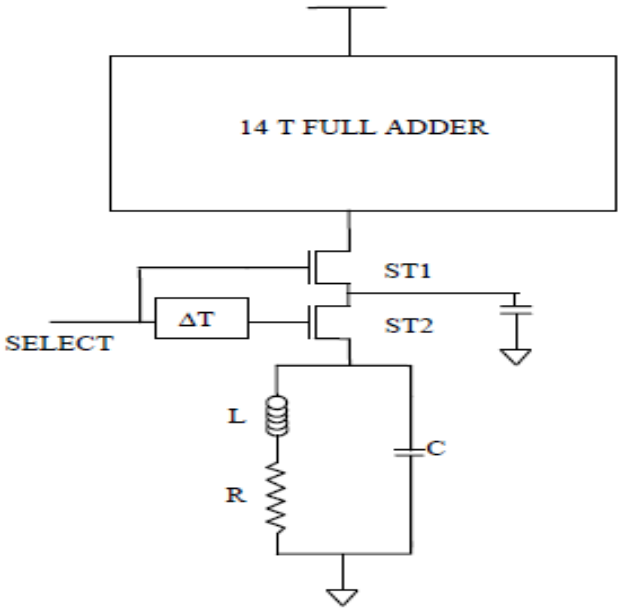

Fig: 2

When adding the `ones' column, we say 1 and 1 is 0, carry 1' and write a 0 under the `ones' column. When we add the `twos' column, we say 1 and 1 is 0, carry 1, plus the carry from the `ones', is 1, carry 1. We write a 1 under the `twos' column and carry 1 to the `fours' column. Here we say 0 and 1 is 1, plus the carry from the `twos' column, is 0, carry 1. We write the 0 in the `fours' column and carry 1, which we write under the `eights' column. In other words, the truth table for a `full adder' able to handle carries as well as two binary digits

2.1 Typical design flow

Typical design flow for designing VLSI circuits is shown in the tool flow diagram.

This design flow is typically used by designers who use HDLs. In any design, specification are first. Specification describes the functionality, interface and overall architecture of the digital circuit to be designed. At this point, architects need not think about how they will implement their circuit. A behavioral description is then created to analyze the design in terms of functionality, performances and other high level issues. The behavioral description is manually converted to an RTL (Register Transfer Level) description in an HDL. The designer has to describe the data flow that will implement the desired digital circuit. From this point onward the design process is done with assistance of CAD tools.

Logic synthesis tools convert the RTL description to a gate level netlist. A gate level net list is a description of the circuit in terms of gates and connections between them. The gate level net list is input to an automatic place and route tool, which creates a layout. The layout is verified and then fabricated on a chip. Thus most digital design activity is concentrated on manually optimizing the RTL description of the circuit. After the RTL description is frozen, CAD tools are available to assist the designer in further process Designing at RTL level has shrunk design cycle times from years to a few months.

2.2 Ground bounce noise

The high edge speeds and clock frequencies of advanced CMOS technology can produce unwanted oscillations during logic level transitions resulting in random logic bit errors. Designers can spend countless hours searching for the causes of these errors and might completely overlook the effects that picofarad capacitance and nanohenry inductance in ground loop circuits can have on the digital IC power supply ground potential. Voltage drops across these small, reactive component elements can result in ground level shifts or "bounce." The bounce, when added to the device logic level, may be sufficient to erroneously toggle a flip-flop in a neighboring or succeeding logic stage. Fortunately, with an understanding of what influences ground bounce, you can measure it and take corrective action.

Figure 1 is a simplified model of a digital circuit. LP is the inductance of the IC package, which includes the leadframe and bond wires. This can be as large as 20 nH for dual inline package styles. Lc is the inductance of the PCB trace between C1 and the power supply bypass capacitor (typically 0.1 µF). Depending on board layout, Lc can be up to 100 nH. CL is the distributed load capacitance between the PCB trace on the output pin and ground. The load capacitance, which varies with board design, is typically 50 pF. During logic level transitions, the rapid charging and discharging of CL results in an inductive L(di/dt) voltage drop across LPVCC and LPGND. Voltage drop across LPGND causes the IC ground potential to rise above the

power supply ground potential. Other ICs may see this effect as a logic change on the output of the device. When the IC input returns high, ground bounce of the opposite polarity occurs due to the voltage drop across LPVCC.

2.3 Forward body bias

Forward body biasing is a promising approach for realizing optimum threshold-voltage (V_{TH}) scaling in the era when gate dielectric thickness can no longer be scaled down. This is confirmed experimentally and by simulation of a 10-nm gate length MOSFET. Because forward body bias (*VF*) decreases the depletion width (X_{DEP}) in the channel region, it reduces V_{TH} roll off significantly. MOSFET performance is maximized under forward body bias with steep retrograde channel doping, and such channel doping profiles are required to accomplish good short-channel behavior (small X_{DEP}) at low V_{TH} notwithstanding body bias; therefore, the combination of forward body biasing with steep retrograde channel doping profile can extend the scaling limit of conventional bulk-Si CMOS technology to 10-nm gate length MOSFET. Considering forward biased p-n junction current, parasitic bipolar transistor, and CMOS latch-up phenomena, the upper limit for |*VF*| should be set at 0.6-0.7 V, which is sufficient to realize significant advantages of forward body biasing.

3. Pre layout simulation

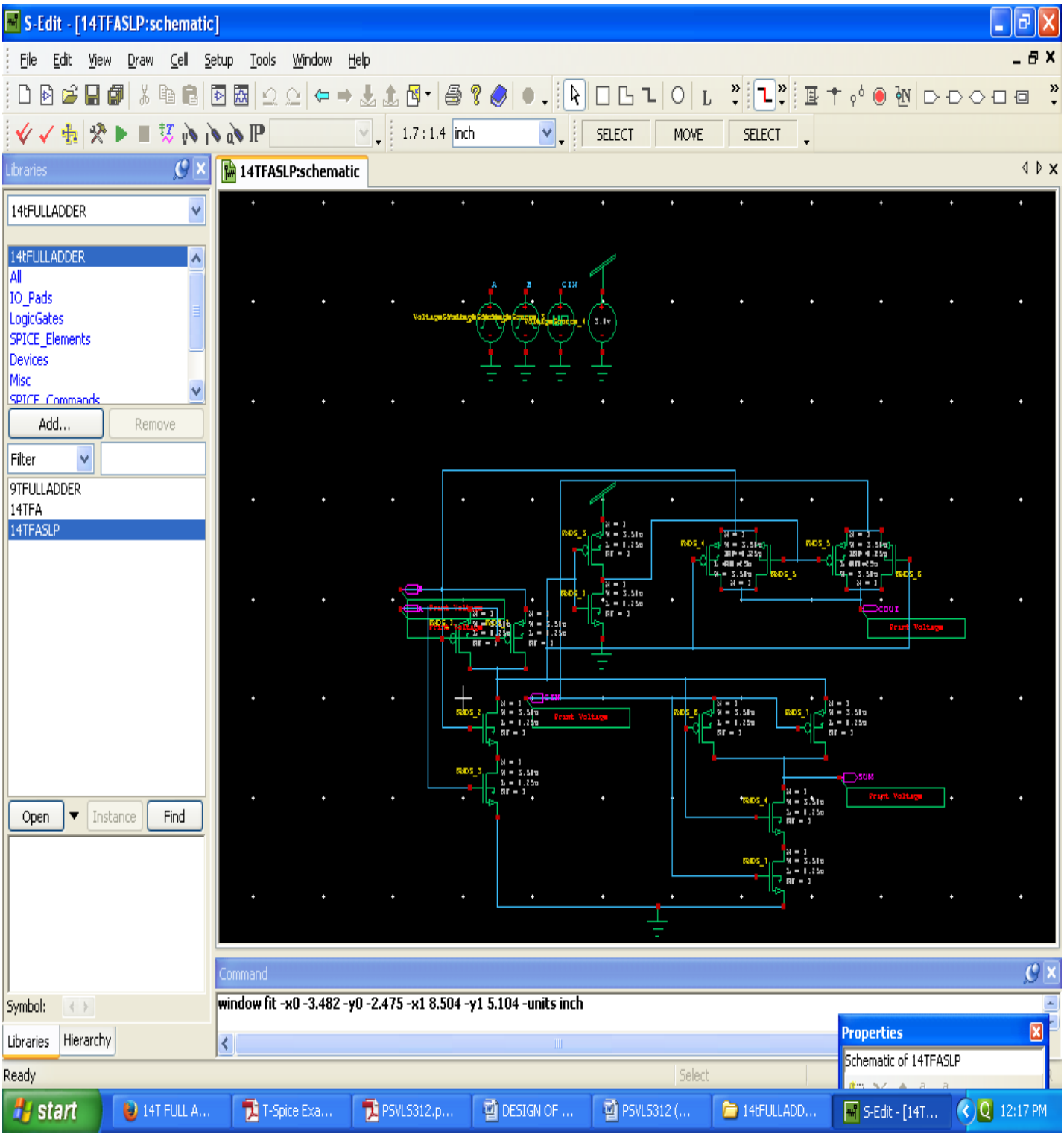

Fig: 3

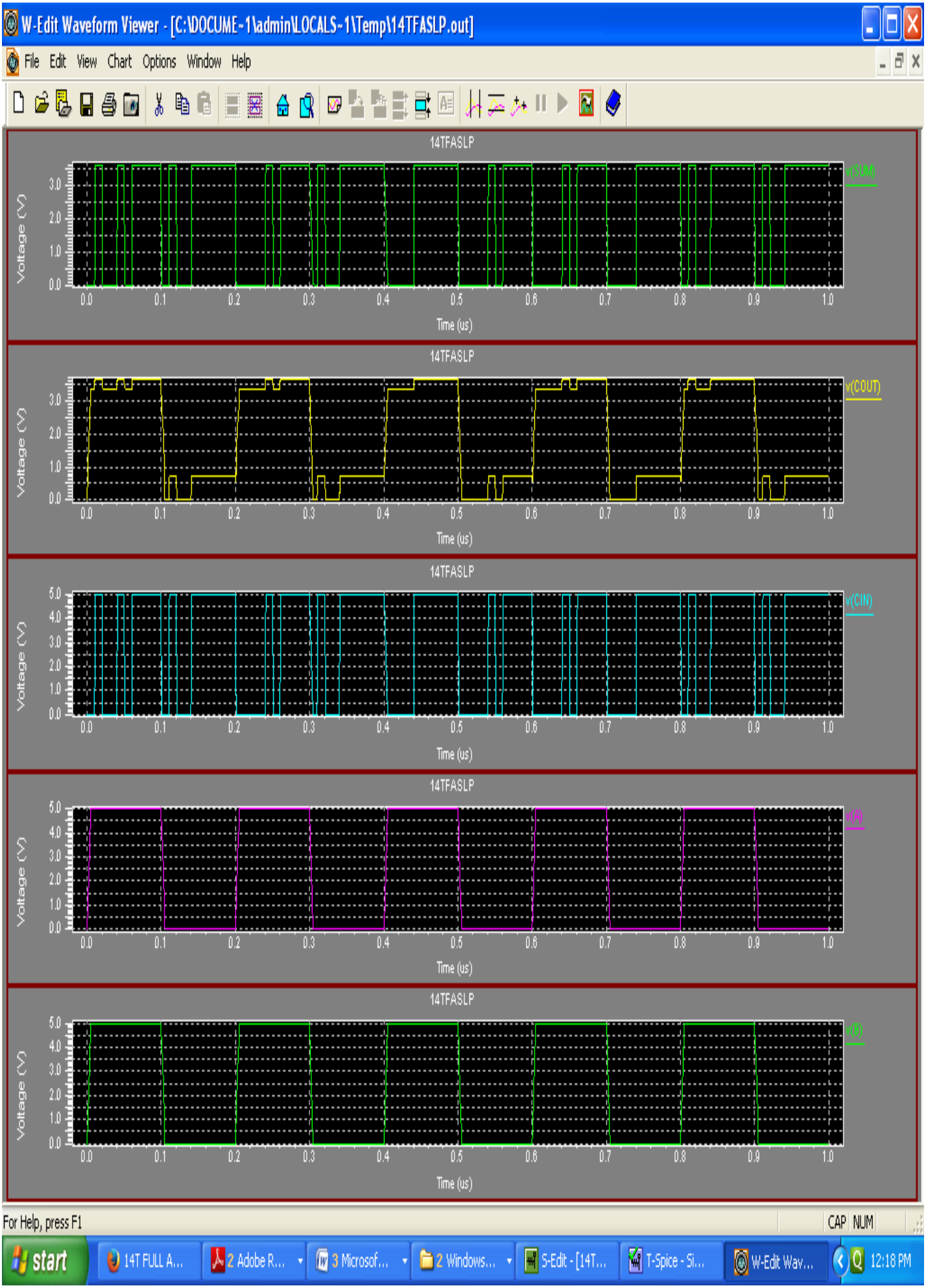
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Fig: 4

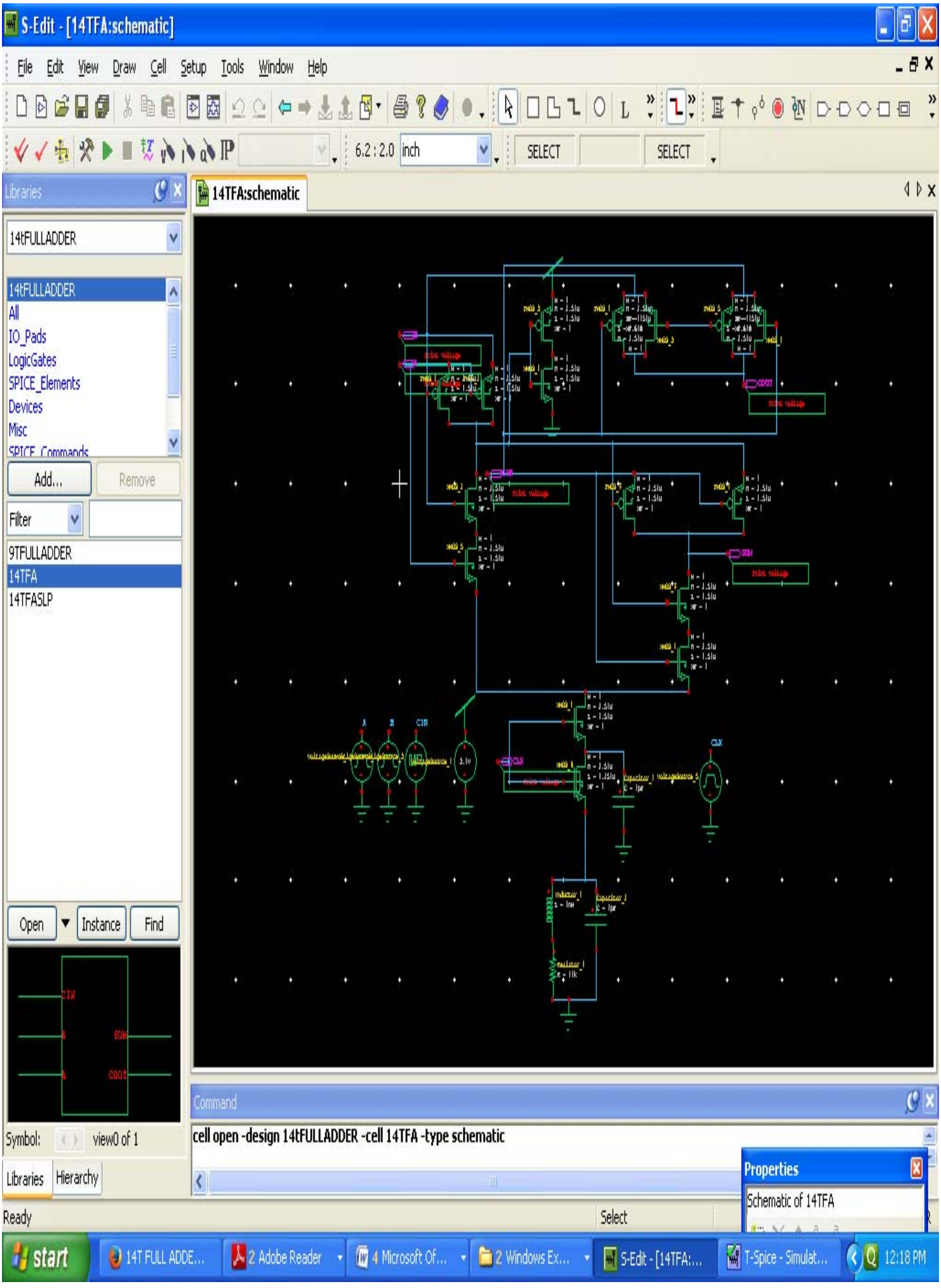
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Fig: 5

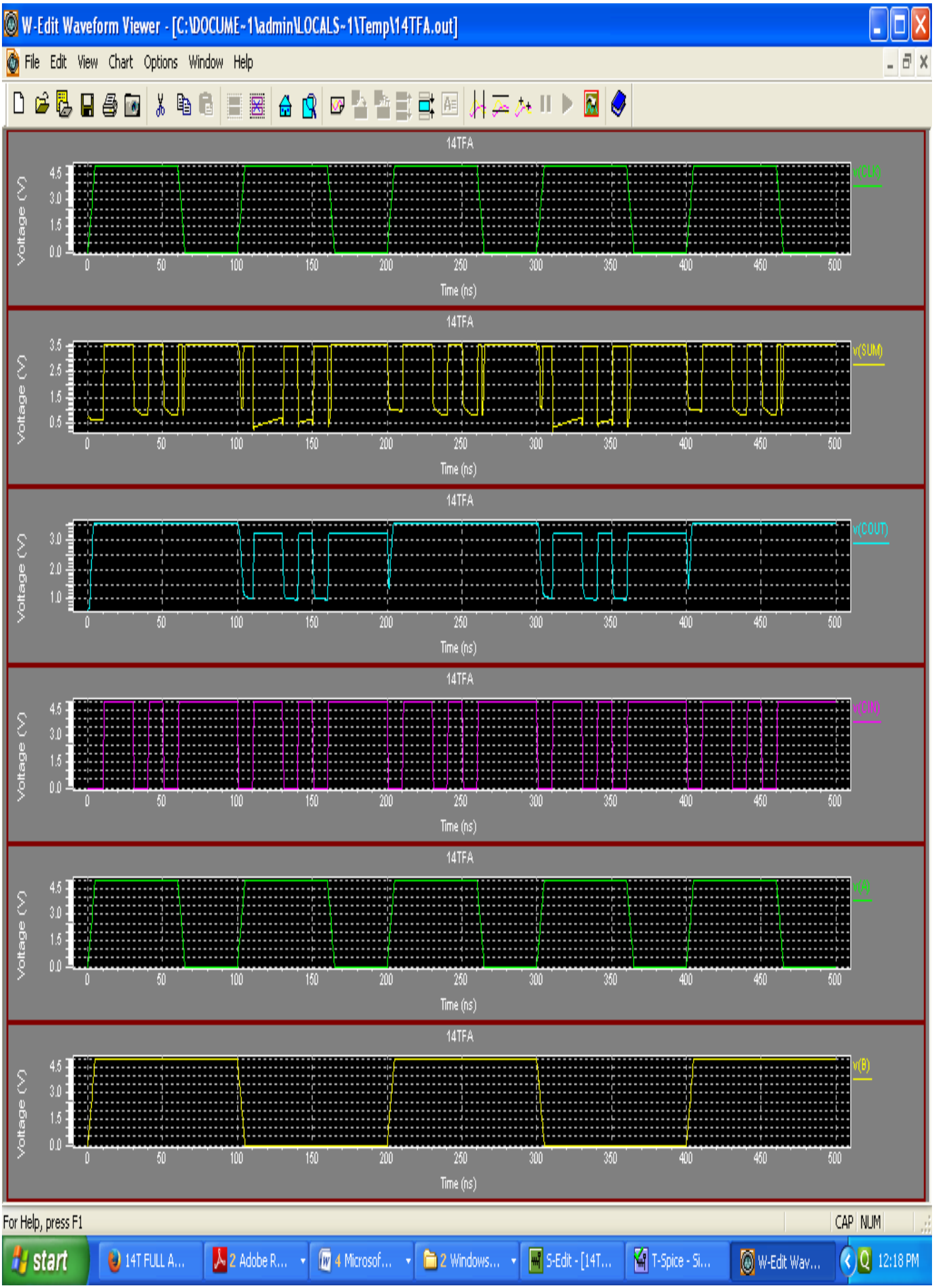
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Fig: 6

4. Conclusion

In this paper we proposed a modified 14T Adder for microprocessor and arithmetic logic circuit with low ground bounce noise and reduce leakage power. Here we have used high performance power gating technique to reduced activepower, leakage power, leakage current and ground bounce noise. The leakage current up to 80% and leakage power upto 32%. The ground bounce noise is reduced to up to 90% and active power is reduced up to 54.39%. The proposed modified 14T adder is operated at various voltages andvarious temperatures'.

5. References

1. Jin-Fa Lin, Yin-Tsung Hwang, Ming-HwaSheu. Low Power 10-Transistor Full Adder Design Based on Degenerate Pass Transistor Logic, IEEE, 2012.
2. Mohammad Hossein Moaiyeri, Reza Faghih Mirzaee, Keivan Navi. Two New Low-Power and High-Performance Full Adders, Journal of Computers, 2009, 4(2).
3. Navi K, Kavehei O, Rouholamini M, Sahafi A, Mehrabi S, Dadkhai N. Low-Power and High- Performance 1-bit CMOS Full Adder Cell, Journal of Computers, Academy Press, 2008, 3(2).
4. Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, Jin-Gung Chung. Low Power Full Adder Using 8T Structure, IEEE Transactions on Circuits and Systems – II: Express Briefs, 2004, 51(7).
5. Karthik Reddy G. Low power-area designs of 1bit full adder in cadence virtuoso platform, International Journal of VLSI design & Communication Systems (VLSICS) 2013, 4(4).