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Design of step-up converter for a constant output in a high power design

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Abstract
In this paper an improved ZCT interleaved boost converter topology is introduced. The proposed interleaved boost converter is embedded of main inductor and an active auxiliary circuit. The proposed converter has significant advantages over the similar soft switching converters. The size of the auxiliary inductor is reduced, and we can obtain higher efficiency. The prototype for the proposed converter was developed with an input of 415V ac power supply feeding a resistive output load of 33 kilo watts. In addition, the advantages like fewer structure complications, lower cost, higher power density and higher efficiency can be found in the proposed converter.

Keywords: boost converter, interleaved techniques, soft switching, zero-current transition.

1. Introduction
The industry nowadays moving toward more efficient high power designs and more efficient electronics has led to the development of the Switch Mode Power Supply (SMPS). There are several topologies commonly used to implement SMPS. In several technical applications, there is a requirement to convert a DC source voltage into a variable-voltage DC output. A DC to DC voltage can be obtained using simply a DC-DC switching converter and is simply known as a DC Converter. AC transformer with a continuously variable turn's ratio is similar to a DC converter. It can be used to step down or step up a DC voltage source, as a transformer.

In the current market field we can find many high power Switch Mode Power Supply (SMPS) module, but the power density and efficiency is still less. Hence the demand for higher efficiency with smaller design is in very much need for the current and the future world. High-switching-frequency operation is necessary to achieve small size of the converter. However, the switching loss will increase as the switching frequency is increased. To solve this problem, soft switching techniques are necessary. The zero-voltage-switched (ZVS) technique and zero-current-switched (ZCS) technique are two commonly used soft switching methods [2]. By implementing these techniques, either voltage or current is zero during switching transitions, which largely reduces the switching loss and increases the efficiency and also increases the reliability of the power supplies.

The selection of the soft-switching technique, i.e., ZCS or ZVS, these considered technique's is the technology of the semiconductor device that is accounted and will be used. For instance, when commutated under ZVS the Power MOSFETSs present a better performance, as when operating in ZCS they exhibit turn-on capacitive losses with increasing the switching losses and EMI. On the other hand, the IGBTs present better results when are commutated under ZCS which can avoid their lath up and the turn-off losses caused by the tail current. However, the ZCS techniques suffers from some drawbacks such as, a significant voltage stress on the main diode, which increases the conduction losses, and the presence of the resonant inductor in series with the main switch, which increases the magnetic losses [3].

2. Proposed Topology
Fig 1, is the proposed block diagram, the three phase diode bridge rectifier is used to convert the ac line input voltage to the dc value. The circuit consists of an interleaved boost converter. With the help of this interleaving technique, inductor current of interleaved boost

converter can be reduced. Thus result in reducing inductor size. And by using a main inductor we can increase the effective switching frequency further reducing the size of the auxiliary inductors.

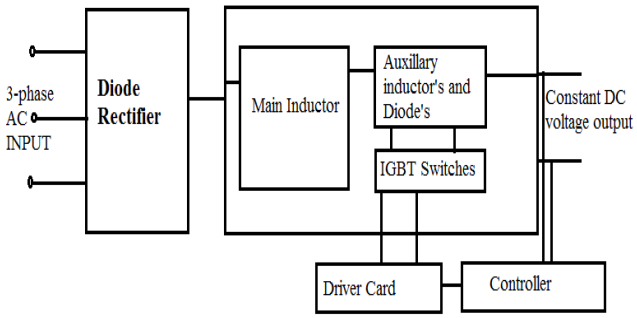

Fig 1: Block Diagram of AC-DC Converter

Fig 2, The main switches of the converter, Q1 and Q2 are gated with 180^0 phase shift with identical frequencies and duty ratios. In SMPS a semiconductor switch (IGBT) is used, which offers very low resistance at the ON state, minimizing conduction loss, and very high resistance at the OFF state, blocking the conduction. A low-pass filter using non-dissipative passive components such as inductors and capacitors is placed after the semiconductor switch, to provide constant DC output voltage. The semiconductor switches (IGBT) used to implement switch mode power supplies are continuously switched on and off at high frequencies (20 kHz) to transfer electrical energy from the input to the output through the passive components.

The main inductor is added in series with interleaved boost converter to reduce the peak current which reduces the turn-on losses, and the interleaved technique reduces the switching frequency by half which reduces size of the auxiliary inductors. Hence we can have higher efficiency and higher power density with reduced size at high power designs. Using of nano-crystalline core for inductor components reduces the size of overall circuit.

The output voltage is controlled by varying the duty cycle, frequency or phase of the semiconductor device's transition periods. As the switching frequency is inversely proportional to the size of the passive components, a high switching frequency result's in smaller sizes for magnetics and capacitors.

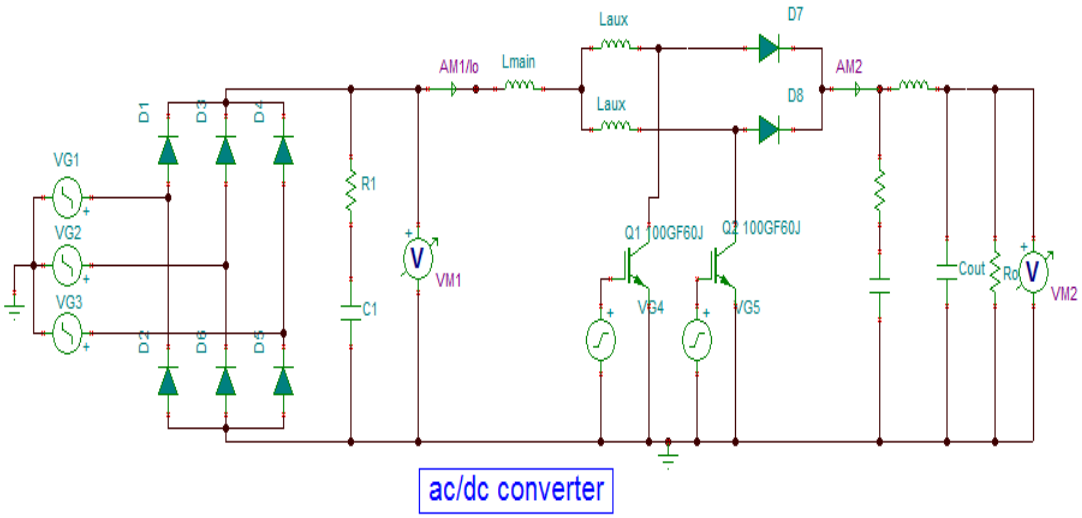

Fig 2: Proposed circuit for AC-DC converter.

3. Design Procedure

The design procedure for the proposed soft switched interleaved boost converter where main inductor operating in continuous conduction mode (CCM) and auxiliary inductor's in discontinuous conduction mode (DCM), are presented in this section.

4. Operating Requirements

Pout (max):	33 kW
V_{in} range:	415 AC
Line frequency range:	50Hz
Output voltage:	650 V_{DC}

5. Switching Frequency

The selection of switching frequency is generally somewhat arbitrary. The switching frequency must such that it should be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. Switching frequency range in most applications is 20 KHz to 300 KHz proves to be an acceptable compromise [4]. In this converter we use a switching frequency of 20 KHz at the main inductor as a compromise between size and efficiency. The value of the inductor will be reasonably small and also distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive.

While the high frequency switching offers the designer a huge advantage for increasing the power density, it adds power losses inside the converter and introduces additional electrical noise. So by using the interleaved boost converter we reduce the switching frequency by using two paralleled auxiliary inductor. And to keep the efficiency high we introduce a main inductor in series with auxiliary inductor which results in continuous conduction mode of operation with good average current sharing and low current ripple, this reduces the inductor size largely and also has higher efficiency.

Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. So we introduce a main inductor which keeps the switching frequency high and also reduce the size of the auxiliary inductors, which reduces the turn-off losses. So we select effective switching frequency: 20kHz and switching frequency at auxiliary inductor: 10kHz

6. Input and Output Parameters

The relationship between the duty cycle and the output/input ratio for interleaved boost converter is.

$V_o = \left(\frac{1}{1-D}\right) \times V_g$ .....(1)

$I_{in} = 58.92A$ .....(2)

$D = 1 - (Vg - Vo)$ .....(3)

Rectified voltage

$Vg = 3\sqrt{2} \times Vm$ .....(4)

Output current

$Io = \mu(1 - D)Iin$ .....(5)

Output power

$Po = Vo \times Io$ .....(6)

$Vo = Io \times Ro$ .....(7)

From the above equation

$R_o = \frac{Vo}{Io}$ .....(8)

7. Selection of Inductors

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak current of the input sinusoid.

$I_{avg} = 58.92A$.....(9)

$I_{pk} = \frac{Iavg}{(1-D)}$ .....(10)

$Irms = Ipk \times \sqrt{(1 - D)}$ .....(11)

$I_{ripple} = \sqrt{I^2_{rms} - I^2_{avg}}$ .....(12)

$\frac{V}{l} = \frac{di}{dt}$ .....(13)

$L_{main} = \frac{(Vin \times D)}{\Delta I \times Fsw}$ .....(14)

$L_{aux} = \frac{Vout \times tp}{2\Delta I}$ .....(15)

Now considering 2% of the ripple output voltage.

$C_{out} = \frac{Iout \times D}{Fsw \times \Delta Vout}$ .....(16)

D = 0.13846
V_g = 560V
I_o = 50.78A
P_o = 33kW
R_o = 13Ω

Componets Value at Converter

I_{avg} = 59.92A
I_{pk} = 68.35A
I_{rms} = 63.46A
I_{ripple} = 23.6A
L_{main} = 163uH
L_{aux} =1.38uH
C_{out} = 168uF

8. Simulation Results

The computer simulation of proposed converter is done using TINA and the results are presented. The simulation result of input voltage and input current is shown in figure 2(a) and figure 2(b) respectively. The simulation result of rectifier output voltage, output voltage, output current, output of pulse generators are shown

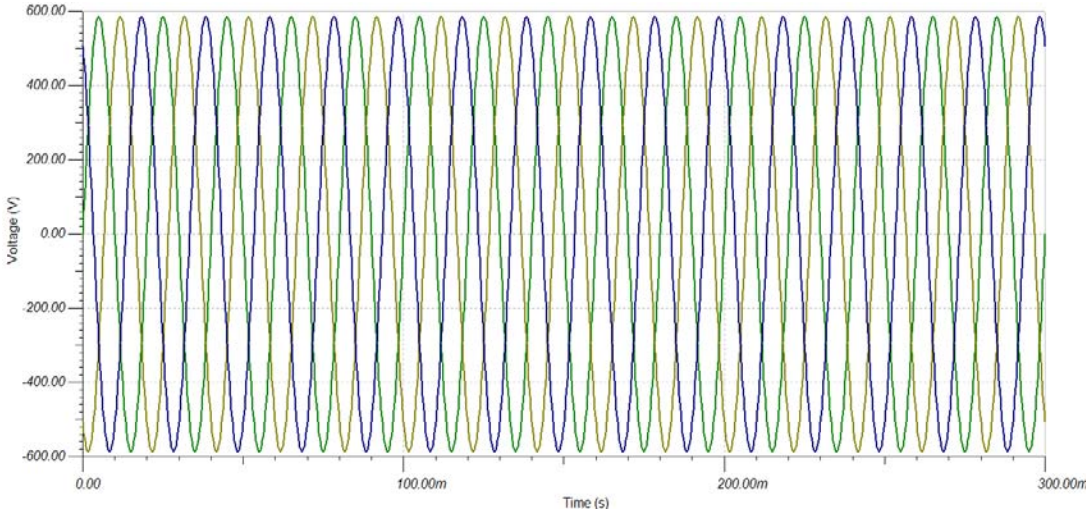

Fig 2(a): Simulation result of input voltage.

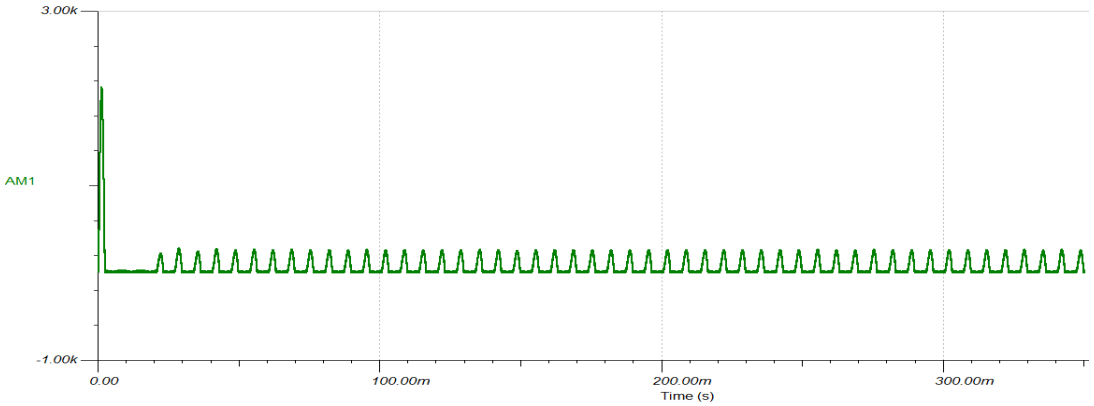

Fig 2(b): Simulation result of input current

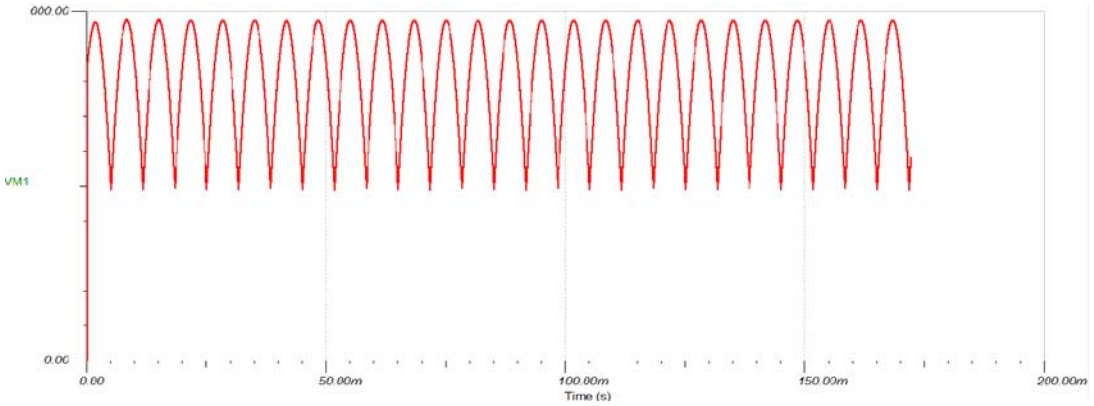

Fig 2(c): Simulation result of rectifier output voltage.

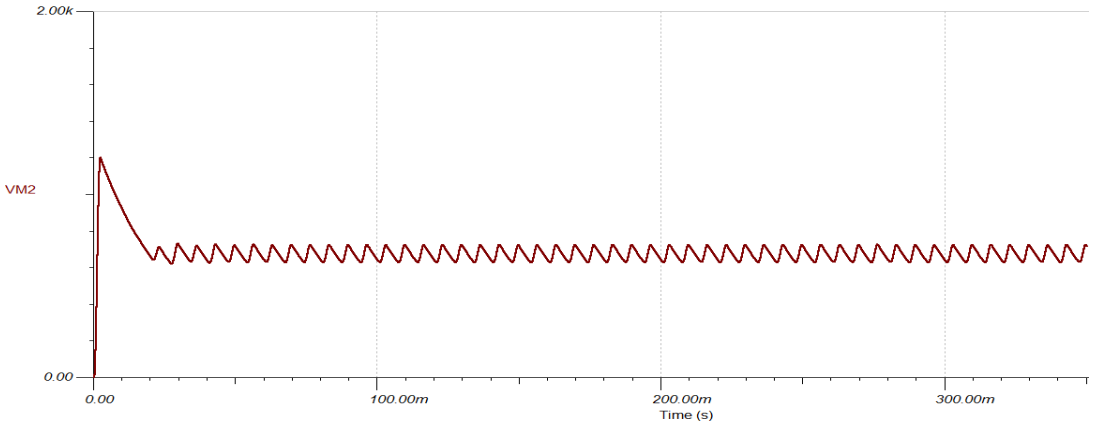

Fig 2(d): Simulation result of output voltage

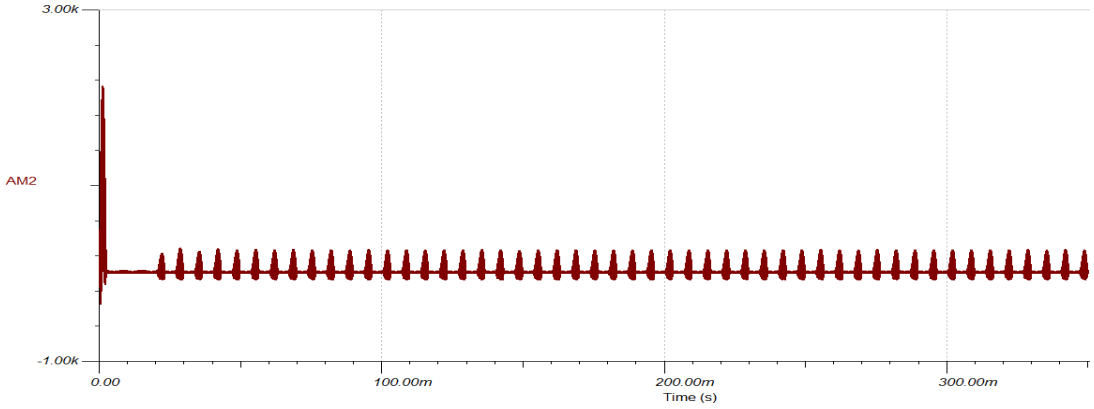

Fig 2(e): Simulation result of output current

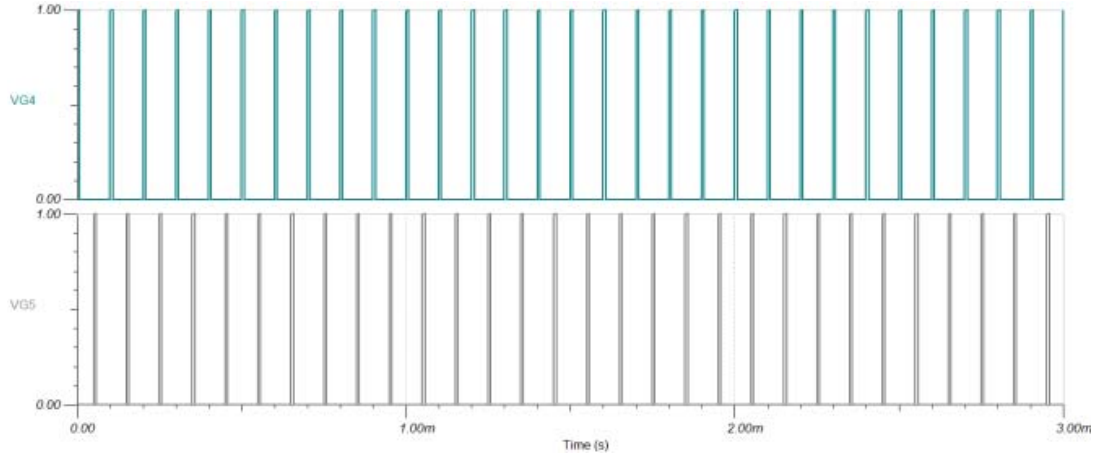

Fig 2(f): Simulation result of pulse generators

9. Conclusion and Future Work

In this paper an improved interleaved boost topology for high power SMPS is introduced. The computer simulation of the converter design has been carried out using TINA-9.exe. From the results, it can be seen that the main switches are turned on and off using soft switching technique. Also, this soft switching of the switches is the main advantage of the proposed topology. The soft switching of the output diodes also reduces switching losses. And also by using main inductor we can reduce the peak current, and hence reduce the size of auxiliary inductors, and we can obtain a constant output voltage, which is very helpful in further aspect of the design. Hence we can obtain higher efficiency and smaller design. The complete design of SMPS is also under progress. The prototype of the proposed topology has been designed and experimental study is under progress.

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