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Design and implementation of LDPC decoder using time domain-AMS processing

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Abstract
At the cost of limited accuracy, analog computation is more energy efficient and area efficient. On other side, digital computation is more versatile and achieves greater benefits from technology scaling. Time Domain analog mixed signal processing (TD-AMS) utilizes both digital and analog computation advantages, and it is better solution which suits in implementing a system on chip and also includes functions which does not require high accuracy, like voice transmitting, image processing, error correction codes etc. An example, a low density parity check (LDPC) decoder is implemented using TD-AMS technique, in Xilinx ISE 14.5 and target family Spartan 3E, Device XC7A100T, speed -3, package:CSG324. Proposed Binary Search TDC is implemented using TD-AMS technique, which achieves less area and less delay compared to conventional TDC.

Keywords: *Analog computation, low-density parity-check (LDPC) code, LDPC decoder, time-to-digital converter (TDC).*

1. Introduction
The rationale behind digitally-assisted analog design is to remove the accuracy burden from the realm of analog design to the digital domain. Reducing the precision of the analog circuitry reduces power consumption significantly, therefore the correction of analog imperfections is implemented in the digital domain, allows less power and faster designs [1]. At this stage the motivating question shall be discussed why TDCs suddenly become popular in mainstream micro-electronics: Modern VLSI technology is mainly driven by digital circuits. The reasons are many, the advantages of digital compared to analog circuits: Atomic digital functions can be realized by very small and simple circuits. This results in a compact and implementation of elementary logic functions are cheap and enables complex and flexible signal processing systems [2]. A comparable complexity design was not feasible with an analog implementation due to area and power consumption but also due to variability and signal integrity.
Flexible means reconfigurable, adjustable or even programmable. Data can be stored easily in digital systems without any loss of information. The design of logic circuits is highly automated which resulting in high design efficiency and productivity. However, the main advantage of digital signal processing is that the inherent robustness of digital signals against any disturbances, i.e. noise and coupling, and also the inherent robustness of digital (logic) circuits against process variations [4].

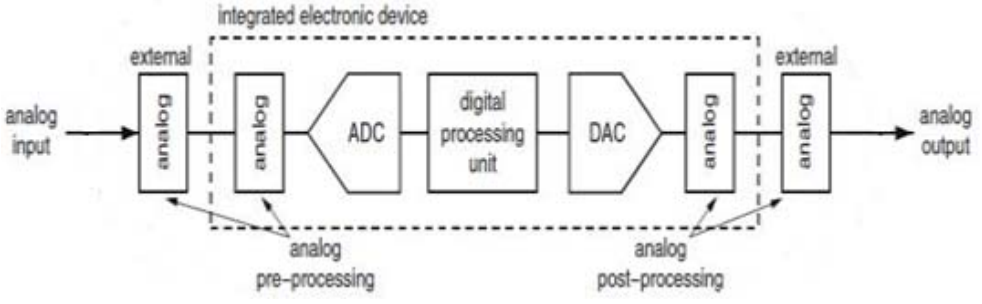

Fig 1: General digital signal processing system

The supply voltage is reduced which accompanied technology scaling, which is dramatically improves the energy efficiency and area efficiency of a digital circuits, which makes the realization of voltage domain analog computation circuits complex. In order to maintain the dynamic range under such a low supply voltage, it is necessary to reduce the mismatches and thermal noise, and that results in large chip area and low power consumption [1].

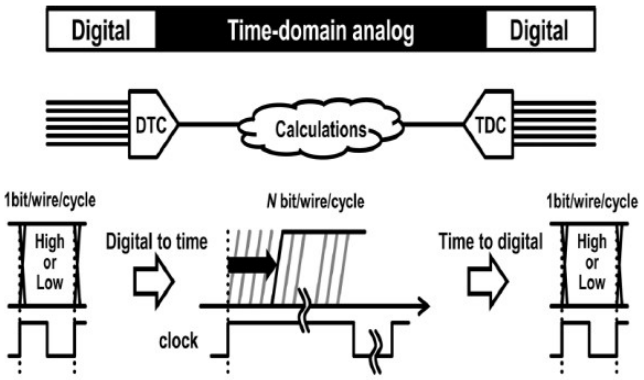

Fig 2: Basic Time Domain-AMS

1. Design and Implementation

Digital to Time Converter

The single-bit DTC circuit diagram and its operation principle are shown in Fig.3 Digital-to-time conversion is analyzed by selecting a signal from delayed or non-delayed time-domain Signals which are originated from clock according to a digital input signal. The DTC is composed of unit delay cells with Tdel delay (DELs), NORs, and inverters [1]. When Din is low, node B remains low and a rising edge of passes through two NORs. On the other hand, when node B is high, the rising edge passes through DEL and also passes to two NORs. As a result, according to Din is high or low, the timing of the rising edge varies Dout by Tdel.

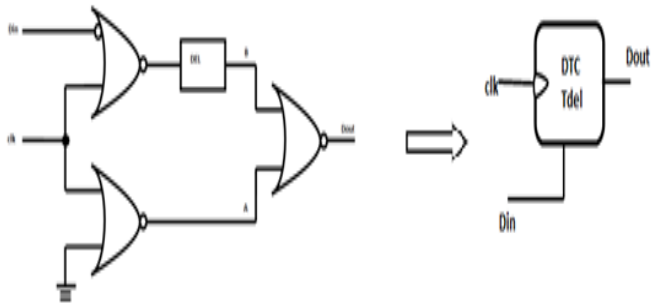

Fig 3: Circuit diagram of 1bit Digital to time Converter

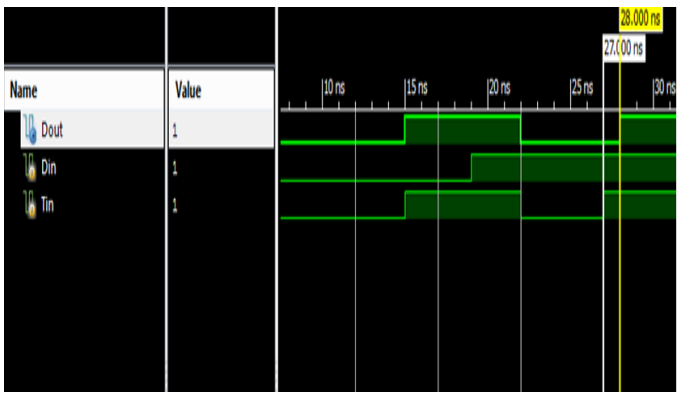

Fig 4: Timing waveform for 1bit DTC

A multiple-bit DTC is composed by cascaded single bit DTCs with binary digital weighted numbers of DELAYs. For example 4bit DTC

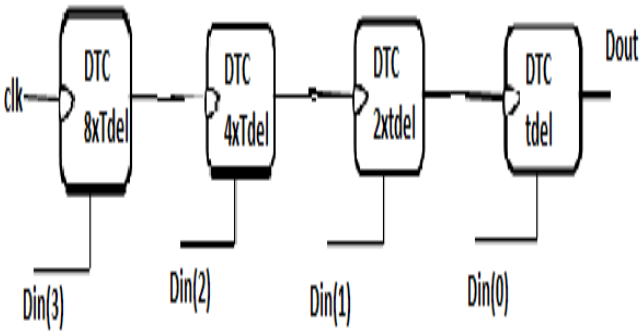

Fig 5: Proposed 4bit DTC circuit diagram

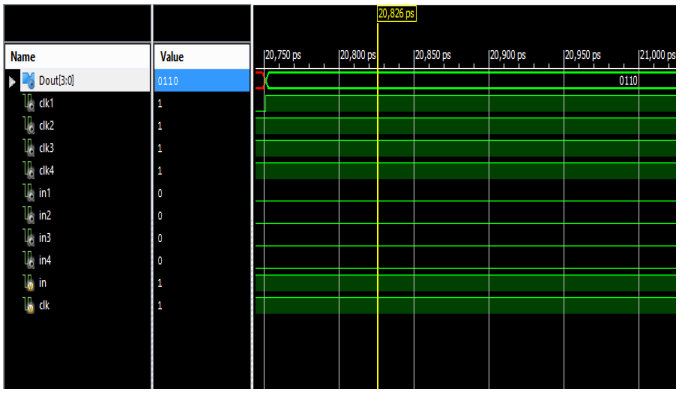

Fig 6: Timing waveform for 3bit DTC diagram

Conventional TDC and Its Operation

The reference clock which is in a more common signal, sense an arbitrary start signal is delayed along the delay line. As the stop signal arrives the delayed versions of the input signal are sampled in parallel. Either latches or flip-flops can be used as sampling elements. The sampling process freezes the state of the delay line at the particular instance where the clock signal occurs [7]. These results in a thermometer code because all delay stages have been already passed by the start signal give a logic HIGH value at the outputs of the sampling elements, all delay stages which have not been passed by the input signal yet shows the LOW value. The position of the HIGH LOW transition, here in this thermometer code indicates how far the input signal can propagate during the time interval spanned by the input and the clock signal. Therefore this transition is a measure for the time interval.

The basic delay-line TDC implementation is shown in Fig. 7. The input signal ripples along a buffer chain that produces the delayed input signals [7]. Flip-flops are connected to the delay elements which are outputs and sample the state of the delay line on the clk signal rising edge. The clk signal drives a more number of flip-flops so a buffer-tree (not shown) is required. Any skew in buffer-tree directly contributes to the non-linearity of the Time to Digital converter characteristics.

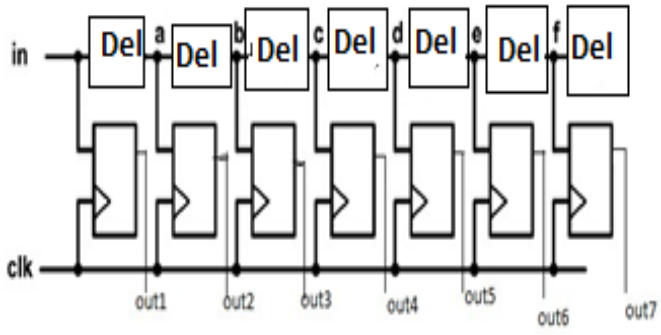

Fig 7: Delay based conventional TDC circuit diagram

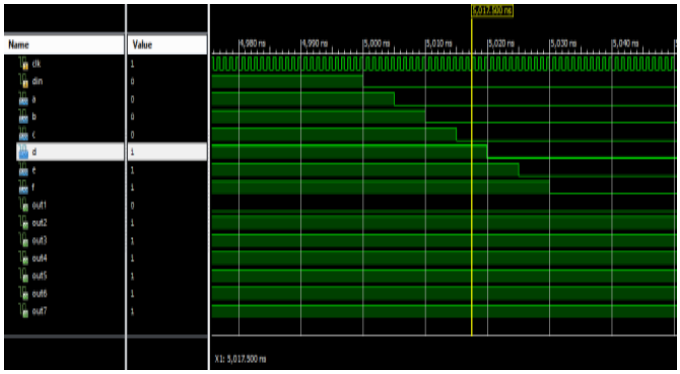

Fig 8: Timing diagram for delay based conventional TDC

Binary Search TDC

TDCs are used extensively now a days in research fields and in all digital PLLs in wireless transceivers and so on, because the TDC can gain the complete benefits of deep submicron CMOS process. Before explanation of binary search TDC (BS-TDC) proposed circuit just briefly describe a conventional TDC, in which it is composed of delay chain and the flipflops, in other words, the required number of flip-flops increases extremely based on n bits, which is leads to increase in more area and more delay. In order to reduce those parameters, the proposed BS-TDC based on binary search algorithm as shown be fig. 9. the n-bit BS-TDC is composed only of n Flipflpos, whereas 2^n-1 FFs used in a conventional TDC, because the area and the power for FFs are dominant in TDCs, reducing FFs directly results in area and power reduction. Although a binary-search approach is commonly applied in voltage-domain ADCs.

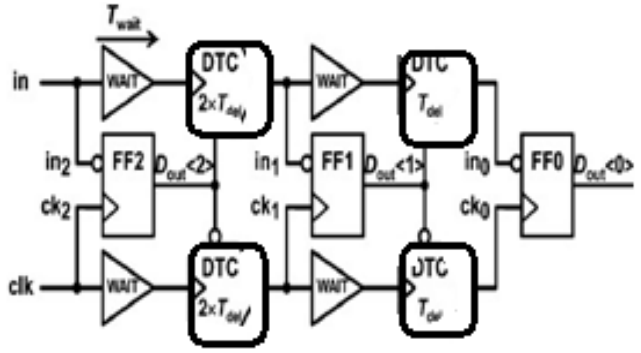

Fig 9: Circuit diagram of the Binary search TDC

Proposed Binary search TDC

The above fig. 9 Binary search TDC is logically incorrect, the corrected circuit and timing diagram of proposed Binary search TDC is shown below

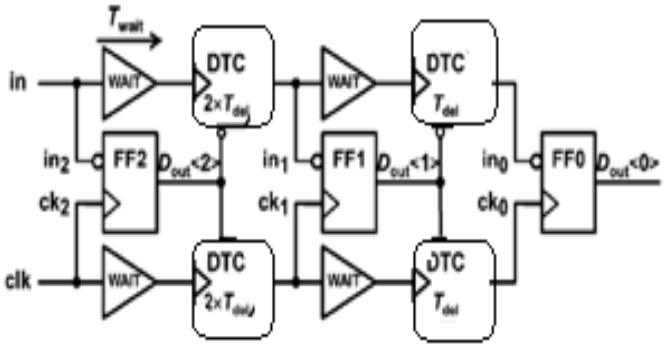

Fig 10: Circuit diagram of the new proposed Binary search TDC

Fig 11: Timing waveform for new proposed binary search TDC

Accuracy of DTC and TDC

The DTC and TDC accuracy with simulation of the circuit show in fig.11 A 1b digital input of DTC is converted into time domain signal and TDC signal is converted to digital output Dout. Based on clock signal of DTC and another input 011 taken as input to full range of the DTC [4]. Then the output of TDC Dout will be high. But the digital logic should not mismatch, if it so error occurrence will appear.

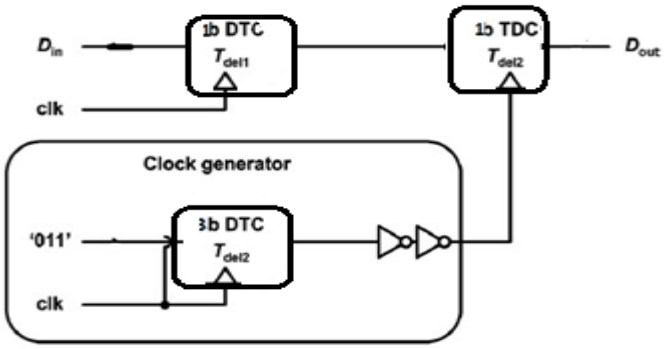

Fig 12: Circuit diagram of accuracy of DTC and TDC

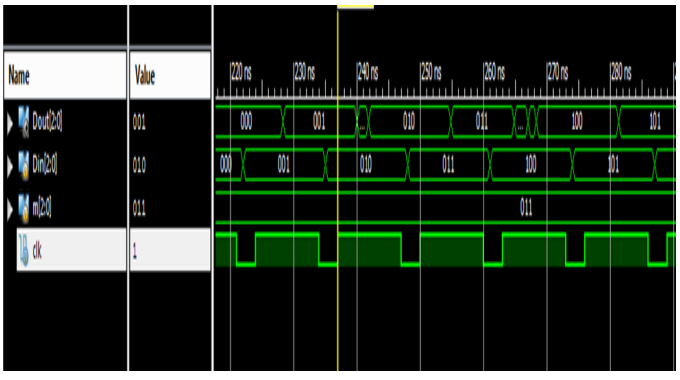

Fig 16: Timing waveform for Accuracy

Summation Circuit

Summation circuit adds two signed and unsigned digital values, its possible to add an offset value so that the digital value is represented in offset binary format, and then, the time-domain adder can handle a negative number. In a digital adder, when a summation result is overflows, it goes to a wrong sign number.

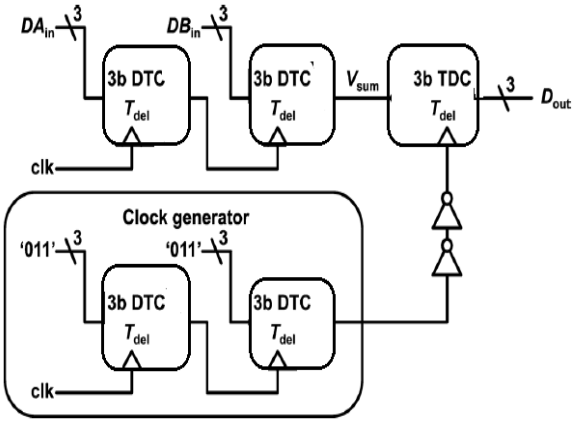

Fig 17: Circuit diagram of Summation

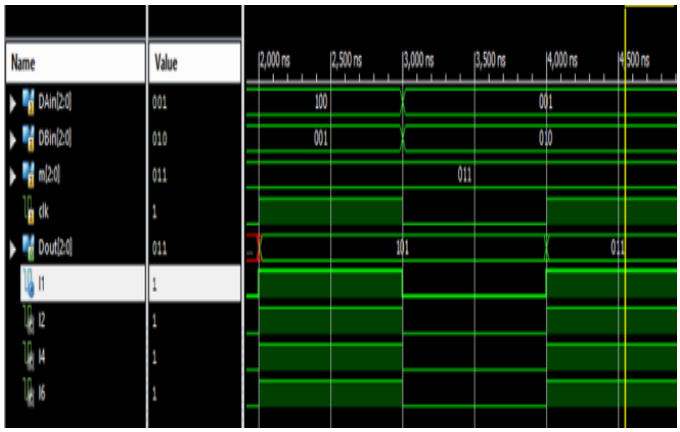

Fig 18: Timing diagram of Summation circuit

Low Density Parity Check Codes

Low-density parity-check codes are a class of linear block code defined by a sparse M x N parity-check matrix, H [5], where N > M and M = N − K. Although LDPC codes can be generalized to non-binary symbols, we consider only binary codes. The parity-check matrix has a small number of „1" entries compared to „0" entries, making it sparse. The number of „1"s in a parity-check matrix row is called the row-weight, k, and the number of „1"s in a column is the column-weight, j. A regular LDPC code is one in which both row and column weights are constant, otherwise, the parity check matrix is irregular. Although a LDPC code is defined by a sparse matrix, a bipartite graph, also known as a Tanner graph, can be used to represent the code. A bipartite graph is a graph whose nodes can be divided into two sets such that each node is connected to a node in the other set. The two sets of nodes in a Tanner graph are called check nodes and variable nodes representing rows and columns respectively [6].

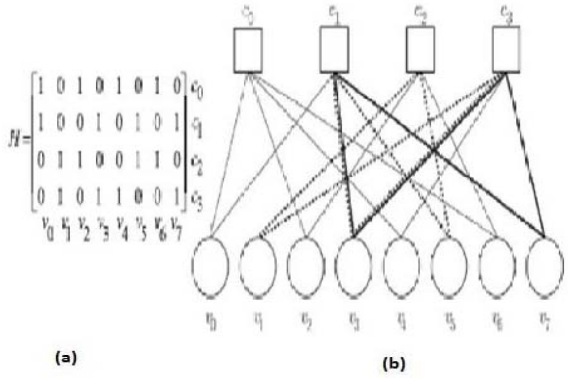

Fig 18: (a) parity check matrix (b) Tanner graph Representation

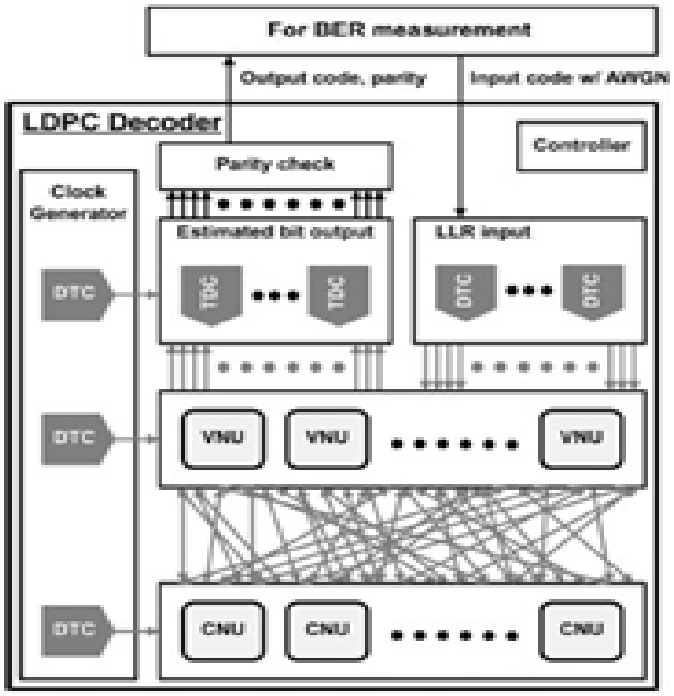

Fig 19: Architecture of LDPC decoder using Time Domain

Tanner graph representation will be reduced to minimum routing congestion and also reduced power consumption [6]. Fig19. illustrates the overall architecture of the implementation (8,4) LDPC decoder leveraging TD-AMS. It is mainly of variable node function units (VNUs) corresponding to (1) and check node function units (CNUs) corresponding to (2). The calculations in the VNUs and CNUs are partitioned into the time domain and digital domain, considering efficiency. The minimum function in the CNU and the summation function in the VNU are executed in the time domain, whereas absolute value (ABS) and XOR function in the CNU are executed in the digital domain.

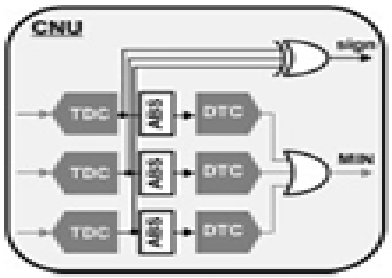

Fig 20: Circuit diagram of CNU

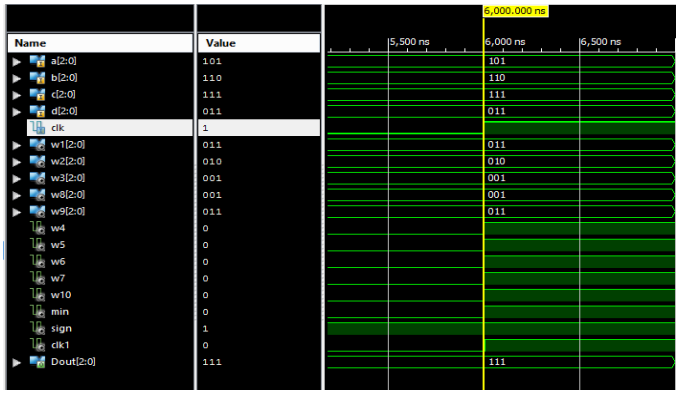

Fig 21: Timing waveform for check node unit

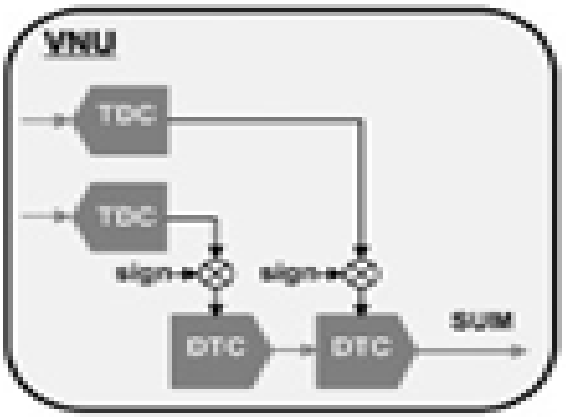

Fig 22: Circuit diagram of VNU

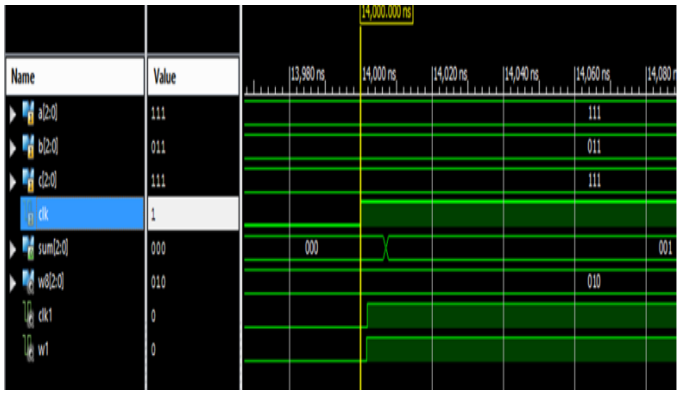

Fig 23: Timing waveform for variable node unit

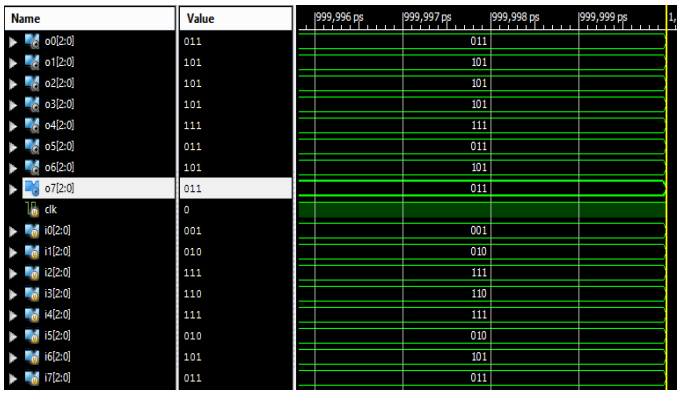

Fig 24: Timing waveform of 3bit LDPC Decoder

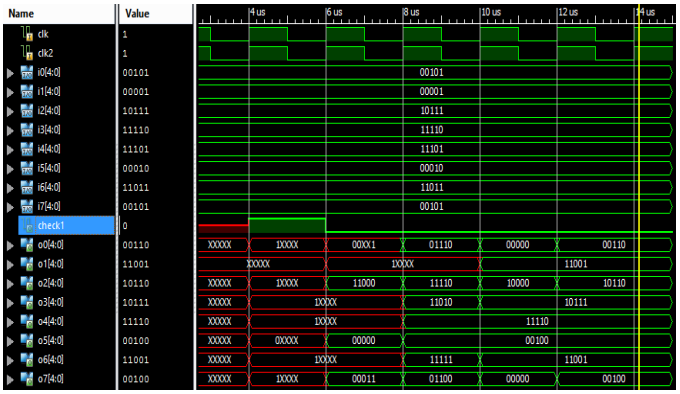

Fig 24: Timing waveform of 5bit LDPC Decoder

Result and Discussion

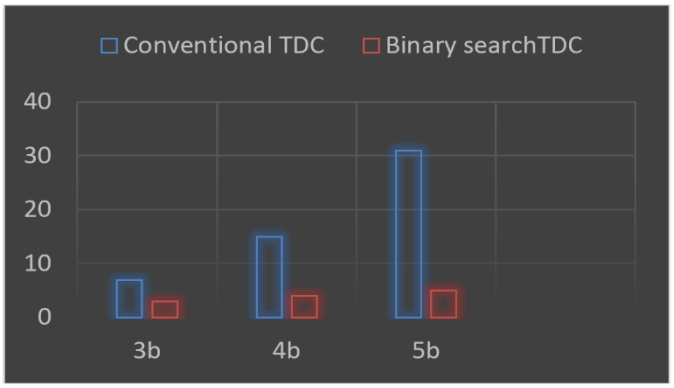

Fig 24: Area Comparison between Conventional TDC and Proposed Binary search TDC

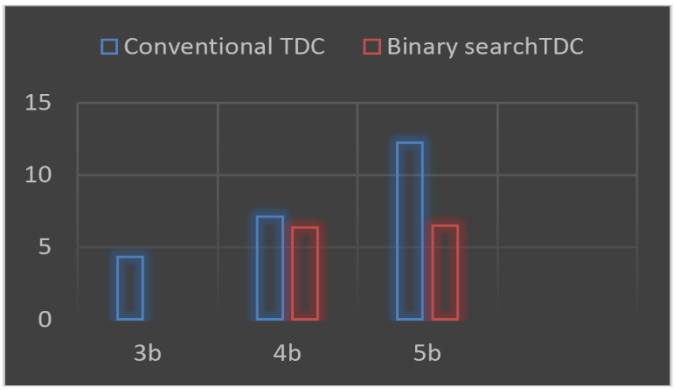

Fig 25: Delay Comparison between Conventional TDC and Proposed Binary search TDC

Table 1: Parameter comparison between conventional TDC and BS-TDC

Types of TDC /parameter	Conventional TDC			Binary search TDC		
Number of bits (n)	3b	4b	5b	3b	4b	5b
Number of LUTs	7	15	31	3	4	5
Delay(ns)	4.32	7.11	12.23	0	6.38	6.5

Conclusions

The large analog circuits are difficult to design, therefore they are reduced to simple functional blocks, which can be used in any digital applications as replaceable functional blocks. This also leads to reduced design complexity and less power consumption. The binary search TDC is proposed which enhances the delay and area efficiencies in applications where high calculation accuracy and accurate

answers are not required, such as error correction, image processing, voice processing.

References

1. Hiroyuki Kobayashi, Kazurori Hashiyoshi. An LDPC Decoder with Time-Domain Analog and Digital Mixed processing. IEEE J of Solid circuits, January, 2014; 49(1).
2. Swann BK. A 100-ps Time Resolution CMOS Time to converter for positron Emission Tomography Imaging Applications, IEEE Journal of Solid-State circuits 2004; 39(11):1839-1852.
3. Lee H, Sodini CG. Anaolgto Digital converters. Digitizing the Analog World, Proceeding of the IEEE, Feb, 2008, 323-33.
4. Jansson JP, mantyniemiand A, Kostamovaana J. A CMOS Time to Digital converter with Better than 10ps single-shot precision, IEEE Journal of Solid State Circuits 2006; 41(6):1286-1296.
5. Juscin CL. An Integrated 16-channel CMOS Time to Digital converter, IEEE Transactions on Nuclear Science, August, 1994, 41.
6. Gallager RG. Low Density Parity Check Codes, Ph.D. dissertation, Massachusetts Inst. technol., Cambridge, MA, USA, 1963.
7. Miyashita D, Yamaki R, Hashi Yoshi K, Kobayashi H, Kousai S, Oowak YY Unekawa. A 10.4 pJ/b (32,8) LDPC Decoder with Time-domain Analog and digital mixed signal processing," in IEEE int. Solid-State Circuit conf. Dig. Tech papers, 2013, 420-421.
8. Hemati S, Banihashemi A, Plett C. A 0.18- m CMOS analog min-sum iterative decoder for a (32, 8) low-density parity-check (LDPC) code, IEEE J. Solid-State Circuits 2006; 41(11):2531-2540.