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High speed Vedic multiplier design and implementation on FPGA

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Abstract
In high speed digital signal processing units arithmetic logic units, multiplier and accumulate units, the multipliers are use as the key block. By increasing constraints on delay, more and more emphasis is being laid on design of faster multiplications. For high speed applications, a huge number of adders or compressors are to be used in multiplications to perform the partial product addition. The Array multiplier, Vedic 4*4 multiplier and 8*8 multiplier are designed, then 16*16 multiplier. These adders are called compressors. Amongst these Vedic multipliers based on Vedic mathematics are presently under focus due to these being one of the fastest and low power multiplier. There are total sixteen sutras in Vedic multiplication in that the 14 number which is nothing but "Urdhva Tiryakbhyam" which is nothing but vertically and crosswise to be the most efficient one in terms of speed. Few of them are presented in this paper giving an insight into their methodology, merits and demerits. Compressor based Vedic Multipliers show considerable improvements in speed and area efficiency.

Keywords: Compressor Adder, Vedic Multiplier, Urdhva Tiryakbhyam sutra (Vertically and crosswise).

1. Introduction
Vedic multipliers are based on Vedic Sutras. In Sanskrit word 'Veda' stands for 'knowledge'. The Vedic mathematics has been divided into sixteen different Sutras which can be applied to any branch of mathematics like algebra, trigonometry, geometry etc. Vedic mathematics is believed to be reconstructed from Vedas by Sri Bharti Krishna Tirathaji between the years 1911 to 1918 [1]. Its methods reduce the complex calculations into simpler ones because they are based on methods similar to working of human mind thereby making them easier. It has been seen that being coherent and symmetrical, they consume lesser power and acquire lower chip area [1]. Designs based on Vedic Mathematics have been used in many applications like ALU, MAC etc. and have shown better results [2-6].

Vedic Mathematics Sutras
Only one Sutra number 14 "Urdhva Tiryakbhyam" has been discussed. There are total Sixteen Sutras in Vedic Multiplier [7]. All these sutras have vast study. These sutras are given below alphabetically with their brief meaning. Discussion of all of them is beyond the scope of this paper.

1. Anurupye Shunyamanyat– If one is in ratio, the other is zero
2. Chalana-Kalanabyham– Differences and Similarities
3. Ekadhikina Purvena– By one more than the previous one
4. Ekanyunena Purvena– By one less than the previous one
5. Gunakasamuchyah– The factors of the sum is equal to the sum of the factors
6. Gunitasamuchyah– The product of the sum is equal to the sum of the product
7. Nikhilam Navatashcaramam Dashatah– All from 9 and the last from 10
8. Paraavartya Yojayet– Transpose and adjust
9. Puranapuranabyham– By the completion or non-completion.
10. Sankalana-vyavakalanabhyam– By addition and by subtraction
11. Shesanyankena Charamena– The remainders by the last digit
12. Shunyam Saamyasamuccaye– When the sum is the same that sum is zero
13. Sopaantyadvayamantyam– The ultimate and twice the penultimate

14. Urdhva Tiryakbyham– Vertically and crosswise.
15. Vyashtisamanstih– Part and Whole
16. Yaavadunam– Whatever the extent to fits deficiency

Urdhva Tiryakbhyam

In signal processing applications multiplication [3] is the most important arithmetic operation. In multiplication all the signal and data processing operations involve. In the multiplication operation as speed is always a constraint, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the main three constraints which determine the performance of the system are speed, area and power requirement. Vedic mathematics [1] was reconstructed by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time. Thus, integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation. The multiplier architecture is based on Urdhva Tiryagbhyam [4] (vertical and cross-wise algorithm) sutra. An illustration of Urdhva Tiryagbhyam sutra is shown in Figure1.

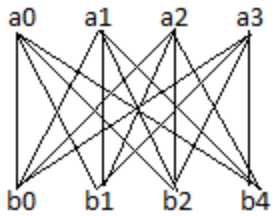

Fig 1: Illustration of Urdhva Tiryagbhyam sutra.

A simple 1-digit binary multiplication is described by AND gate operation. The method can be extended for binary numbers. Using this and UT method 2X2 multiplication for a1a0 and b1b0 is implemented by 2 half adders and resultant bits are r2 (2 bits) r1r0 as shown in Fig. 2. The equations regarding this are given below [9].

r0 (1bit) = a0b0 (1)
r1 (1bit) = a0b1 +a1b0 (2)
r2 (2bit) = b1a1 +c1 (3)
Pro = r2&r1&r0 (4)

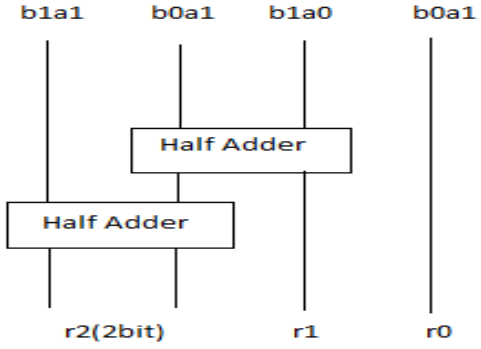

Fig 2: Block diagram for 2X2 Vedic Multiplier

The higher binary multiplications can also be obtained with the help of lower multiplication units and the adder unit. The individual multiplication products are obtained by same partitioning method, ultimately using the 2X2 bit multiplication method. For NXN multiplication unit, we require four N/2 bit multipliers, two N bit full adders, one half adder and N/2 bit full adder to add the sum and carry of half adder. High speed of multiplier depends highly upon speed of adder units used.

Design for Vedic Multiplier with Ripple Carry Adder:-

This architecture can be extended for higher bits like 8, 16, 32 bit multiplications. N bit ripple carry adder consists of N-1 full adder and 1 half adder shown in Fig. 3. This adder is also named as parallel adder because these full and half adders are arranged in parallel in such a way that each adder unit generates a sum bit and carry bit.

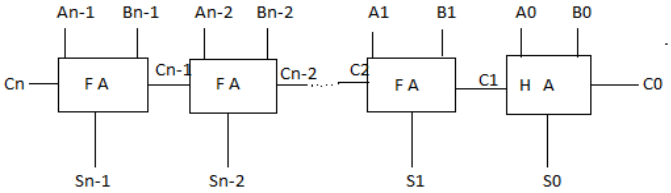

Fig 3: Ripple carry adder

The sum bit is taken as resultant bit and carry is transmitted to next adder unit as an input. The worst case computation time is function of N. In this approach, three 4-bit ripple carry adders are used and the combinational path delay is found to be 13.102 ns. Results are compared with Array and Booth Multiplier and it is observed that the execution time has been reduced for Vedic multiplier and thus proves to be better. Because the carry ripples and each next full adder has to wait for the carry coming from the previous adder, it takes time to propagate. This restricts the speed of this adder and thus proposed design.

The 4*4 Multiplier

The 4*4 multiplication has been done in a single line in Urdhva Tiryagbhyam sutra, whereas in shift and conventional method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier. Consider two 4-bit binary numbers a3a2a1a0 and b3b2b1b0. The partial products (P7P6P5P4P3P2P1P0) generated are given by the following equations:

1. P0= a0b0
2. P1= a0b1 + a1b0
3. P2 = a0b2 + a1b1 + a2b0+ P1
4. P3= a0b3 + a1b2 + a2b1 + a3b0+ P2
5. P4 = a1b3 + a2b2 + a3b1 + P3
6. P5 = a1b2 + a2b1 + P4
7. P6 = a3b3 + P5
8. P7 = carry of P6 (1)

Compressor

Compressors are arithmetic components, similar in principle to parallel counters, but with two distinct differences: (1) they have explicit carry-in and carry-out bits; and (2) there may be some redundancy among the ranks of the sum and carry-output bits. With the increase in number of additions

for higher bit multiplications, a circuit is required that can add them in a single step rather than using multiple full adders and half adders. A new method in Vedic Multiplication is to use the Compressor adder which can add more than three bits at a time as compared to Full adder circuit which can add only 3 bits at a time. Such circuit actually counts number of 1's. It reduces the use of XOR gates and thus minimizes delay and uses MUXs which allowed only a single input to be high at a single time and thus causes decrease in critical delay. Such adders are found to be both high speed as well as low power circuits.

Compressor 5:3

By employing two transistor 2x1 multiplexer in lieu of XOR gates diminishing the critical path delay. The architectures of 5:3 compressor suitable to minimize the stage delay, power dissipation and area. The figure5 shows the block diagram 5:3 Compressor and figure8 shows the RTL diagram of 5:3 Compressor.

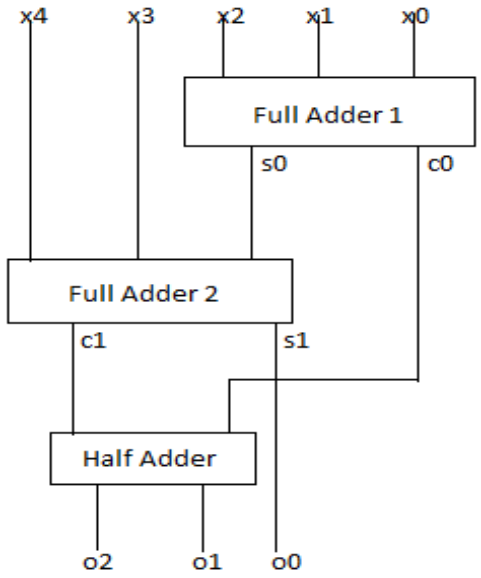

Fig 4: Block Diagram of 5:3 Compressor

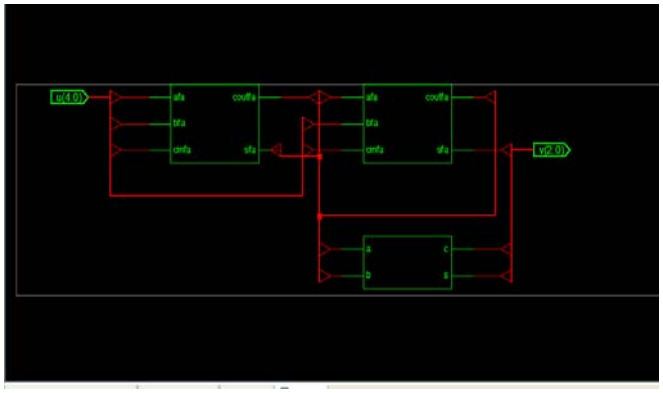

Fig 5: RTL Diagram of 5:3 Compressor

Compressor 6:3

The 6:3 compressor for high speed and low-power multiplier application. The logic of this compressor circuit is totally different from the conventional compressor's logic. It is essentially a single bit adder having six inputs and three outputs and is built most using transmission gates. It is based on the observation that a single bit adder is nothing but the counter of 1's at the input bits. The 6:3 compressor is able to function at a supply voltage of as low as 1 volt. This compressor makes the multipliers faster as compared to the conventional design that have been used 4:2 compressors and 3:2 compressors. The figure8 shows block diagram of 6:3 compressor and figure 7 shows RTL diagram of 6:3 compressor.

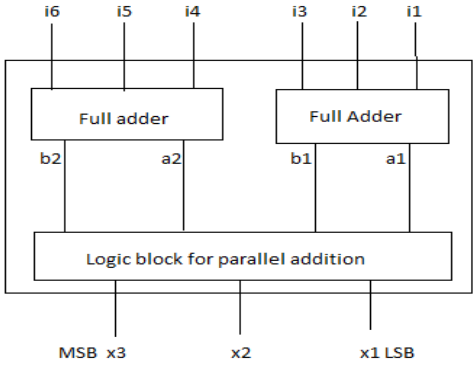

Fig 6: Block diagram of 6:3 compressor

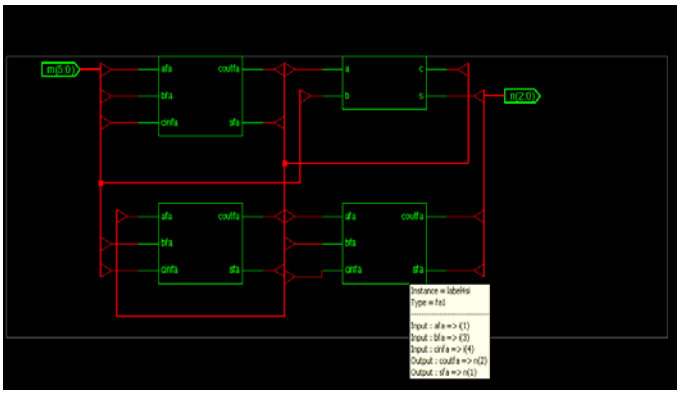

Fig 7: RTL Diagram of 6:3 compressor

Compressor 7:3

A huge number of adders or compressors are to be used to perform the partial product addition. We have reduced the number of adders by introducing special kind of adders that are capable to add five/six/seven bits per decade. These adders are called compressors. Binary counter property has been merged with the compressor property to develop high order compressors. Uses of these compressors permit the reduction of the vertical critical paths. A 16*16 bit multiplier has been developed using these compressors. These compressors make the multipliers faster as compared to the conventional. Figure6 shows the block diagram of 7:3 compressor and figure9 shows the RTL diagram of 7:3 compressor.

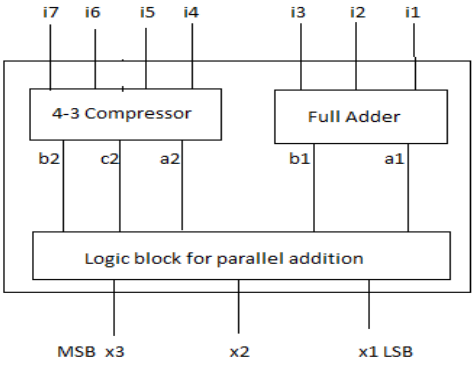

Fig 8: Block diagram of 7:3 compressor

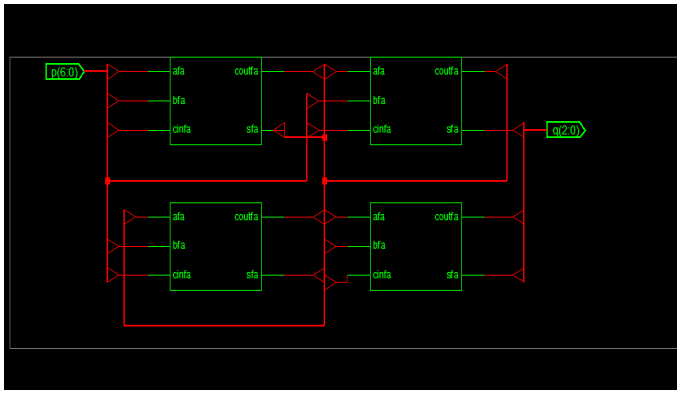

Fig 9: RTL Diagram of 7:3 Compressor

Low Power and High Speed Vedic Multiplier

For designing 16 bit multiplication we use the 7:3 compressor. Fast and low power 16-bit multiplier architecture was proposed by R.K, R.S, S. Sarkar, and Rajesh replacing ripple carry adder with the carry Look ahead adder as in Fig 10. The figure11 shows RTL diagram of 16*16 multiplier by using 7:3compressor.The adder architecture consisted of two parts- Carry generator and Carry propagator. These parts generates the N+1th carry bit with the help of the initial carry and thus this does not need to wait for Nth carry to propagate. Since the carry is generated in advance in this adder, it decreases the carry propagation time and thus this architecture improves the operational speed. A comparison of propagation delay, power dissipation and the number of transistors, made between this architecture, Array multiplier and the Booth radix 4 multiplier, shows that the Vedic multiplier with carry Look ahead adder is better than the other two in speed and power dissipation. But the number of transistors used increases in the proposed architecture. The figure 13 shows the output waveform of 16*16 multiplier by using 7:3 multiplier.

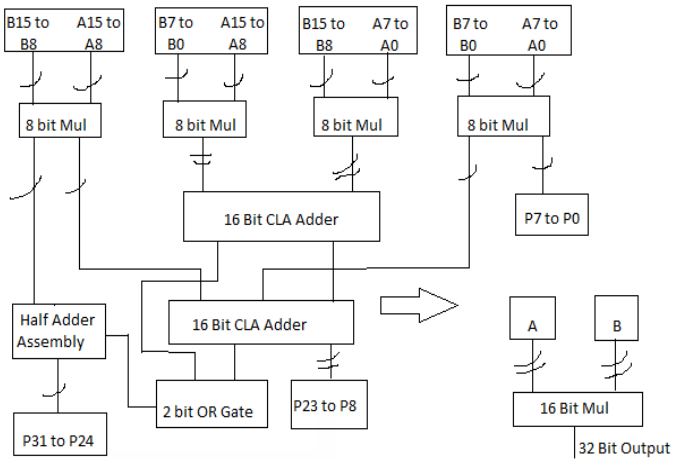

Fig 10: Block diagram for 16-bit Vedic multiplier with CLA adder

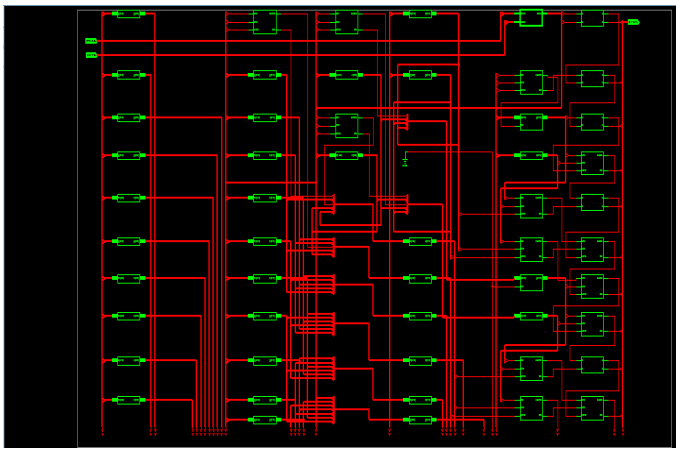

Fig 11: RTL Diagram of 16*16multiplier

Experimental Analysis

Project File:	compress.ise	**Current State:**	Synthesized
Module Name:	mull	**• Errors:**	No Errors
Target Device:	xc3s200-4tq144	**• Warnings:**	2 Warnings
Product Version:	ISE 10.1 - Foundation Simulator	**• Routing Results:**	
Design Goal:	Balanced	**• Timing Constraints:**	
Design Strategy:	Xilinx Default (unlocked)	**• Final Timing Score:**	

compress Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	390	1920	20%
Number of 4 input LUTs	679	3840	17%
Number of bonded IOBs	64	97	65%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon Apr 13 16:40:36 2015	0	2 Warnings	0
Translation Report					
Map Report					
Place and Route Report					
Static Timing Report					
Bitgen Report					

Fig 12: Analysis part of 16*16 multiplier

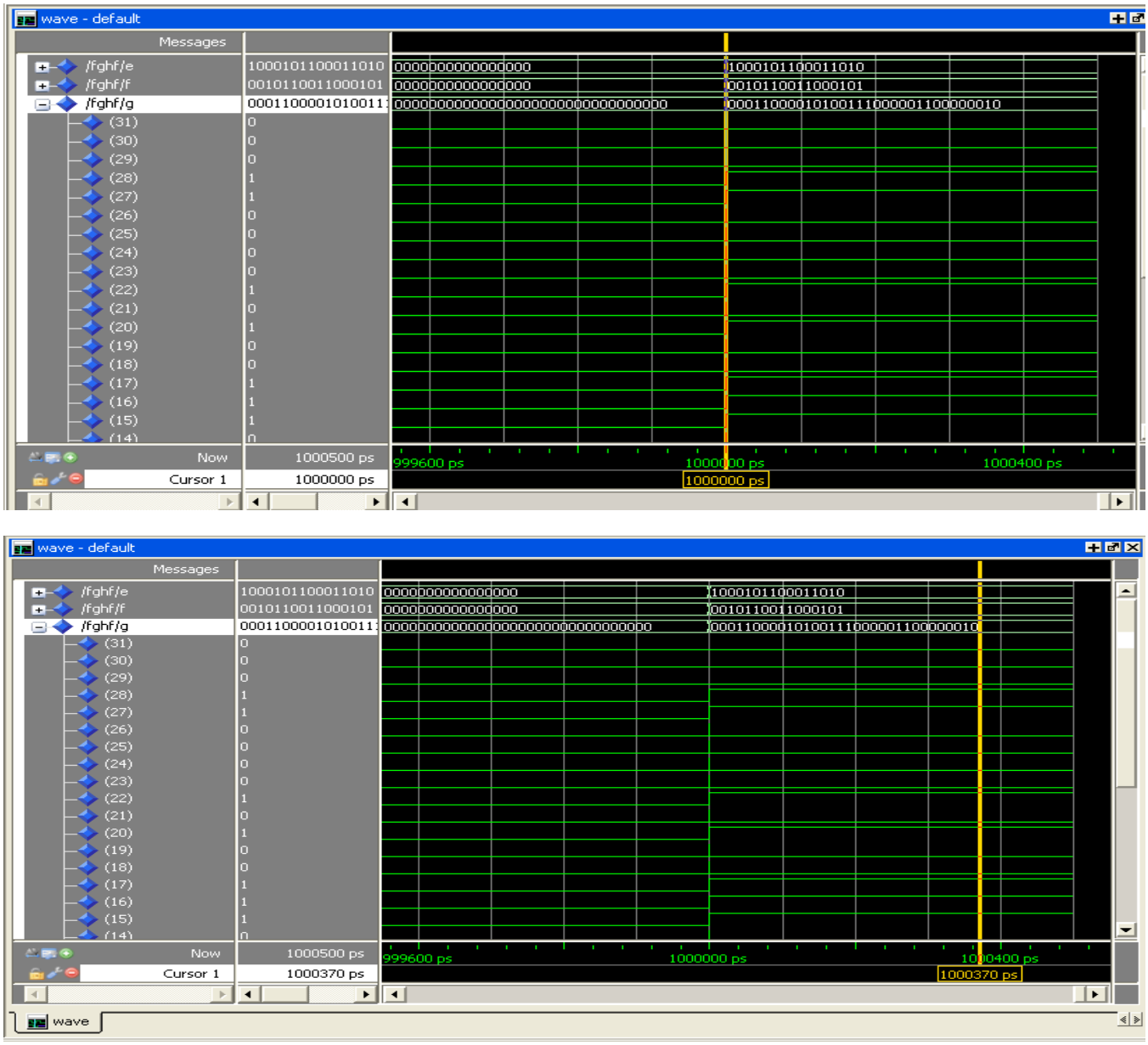

Fig 13: Output Waveform of 16*16 multiplier

Output Format

```
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : NO

Design Statistics
# IOs                              : 64

Cell Usage :
# BELS                             : 679
#       LUT2                       : 175
#       LUT3                       : 211
#       LUT4                       : 293
# IO Buffers                       : 64
#       IBUF                       : 32
#       OBUF                       : 32
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s200tq144-4

 Number of Slices:                      390  out of    1920     20%
 Number of 4 input LUTs:                679  out of    3840     17%
 Number of IOs:                          64
 Number of bonded IOBs:                  64  out of      97     65%
```

Conclusion and Future Scope

This paper presents a novel way of realizing a high speed multiplier using Urdhva Tiryagbhyam sutra and carry skip addition technique. Considering all the designs of it discussed below, Vedic Multiplier is seen to be efficient in speed, power and area in digital designs with respect to other multipliers and implement. In this paper we can conclude that we can easily design 16*16 multiplier by using 7:3 multiplier. We can conclude that the Compressor based Vedic multiplier with Urdhva Tiryakbhyam sutra is seen as a promising technique in terms of speed and area. Ripple carry adders are modified because not all bits have same weight and hardware can be reduced by reducing the number of full adders used. The work can be further extended with the use of such multiplier in arithmetic logical unit, multiply accumulator unit designs and comparing the results with existing designs for the same.

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