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Design of Low-Dropout Regulator

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Abstract
For diminishing the standby power and boosting the effectiveness of battery life time in portable and handheld devices, power management is required. Low Dropout regulator is one of such a power management module. Proposed LDO design converts an input voltage of 1 V to tunable output voltage range of 0.5 V to 0.932 V which is implemented in 90nm technology. The designed LDO has a very less quiescent current of 0.4µA and less dropout voltage of 68mV producing a current efficiency of 99.99%.

Keywords: Low-dropout (LDO) regulator, piecewise curvature corrected BGR, load regulation, quiescent current, area of power MOS transistor, TC – Temperature coefficient.

1. Introduction
Presently, battery equipped gadgets such as cellular telephones, tablets; PDA's and so forth are very requesting in the present business sector pattern. Furthermore, these are liable to be the most imperative products. The one basic parameter that should be considered in longevity of portable devices is battery power. Once the battery power begins depleting and the proficiency of these gadgets decreases. Hence power management needs to be done for these battery operated gadgets. The one such power administration module is regulator. Regulators are of two types namely, linear regulator [1] and switching regulator [10]. In this paper, one example of linear regulator i.e. low-dropout (LDO) regulator is designed. A low-dropout regulator is a DC linear voltage regulator and it can operate with a very less input and output differential voltage. A good LDO must have high tuning range, high current efficiency, low quiescent current I_Q and less dropout
voltage particularly for sub 1-V operation.
Design emphasis of the proposed LDO is on reducing the dropout voltage and reducing the quiescent current [1] – [5]. The LDO design [1] consumes a quiescent current of about 60µA which is quite a high value. If quiescent current increases, the current efficiency decreases. Proposed design is an attempt to reduce the quiescent current and the dropout voltage.

2. Ldo Regulator
A LDO regulator basically consists of mainly four blocks namely a power MOS transistor (M_P), a feedback network, an error amplifier (EA), and a bandgap reference circuit (BGR) as shown in Fig. 1. Some of the advantages of proposed circuit are discussed in the following section.
For sub 1V operation noise suppression must be done because the devices working in sub 1V needs accurate supply. In order to suppress the noise, the proposed LDO architecture consists of rail to rail error amplifier constructed with two stages. The first stage of EA is used to remove the supply noise and the second stage of EA removes the common mode noise present at its inputs. And also power noise cancellation mechanism can be seen at gate of power MOS increases PSR.
In order to compensate for stability i.e. to cancel the non-dominant pole generated by power MOS, a large equivalent resistance of capacitor C_L (R_{SER}) is required to produce a low frequency zero.
For a good LDO the parameters like dropout voltage and quiescent current should be very less. The dropout voltage depends on the maximum load current of the circuit. The dropout voltage can be reduced by choosing very less load current. If dropout voltage is less, it implies the quiescent current also decreases to very low value.

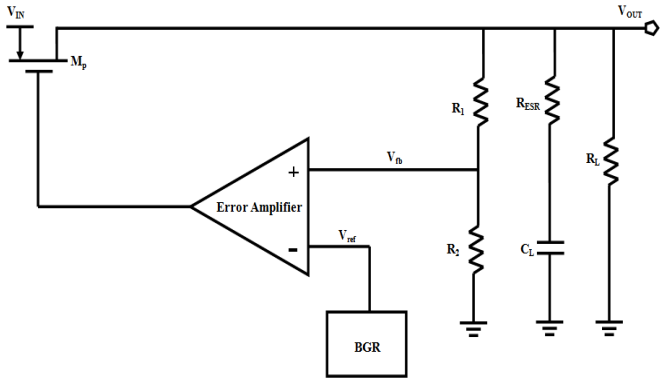

Fig 1: Block diagram of proposed LDO

The power MOS transistor used here consumes more area in the total overall area consumed by the LDO circuit. Hence the size of this power MOS transistor must be reduced. This can be done by increasing the output voltage swing and gain of the rail to rail error amplifier.

3. Design of Ldo

LDO regulator consists of mainly four blocks and designing of all four blocks are explained in the following sections.

A. Error Amplifier

The error amplifier is a rail to rail two stage operational amplifier as shown in Fig.2. The simple rail-to-rail input stage has a p-channel differential pair and an n-channel differential pair is connected in parallel.

The architecture is composed of a bias generator circuit, a constant-transconductance rail-to-rail input stage, a class-AB output stage, a current summing circuit for summing the outputs from NMOS and PMOS amplifiers. The input stage here keeps constant total transconductance over entire common-mode input range and hence maintains very less signal distortion.

In this EA, the current summing circuit is used to convert current gain into voltage gain and to sum the input currents. The class-AB output stage with high capability of driving can obtain wide swing at the output. Here in order to achieve the phase margin of amplifier greater than 60^0, the compensation capacitor is chosen as 800 fF.

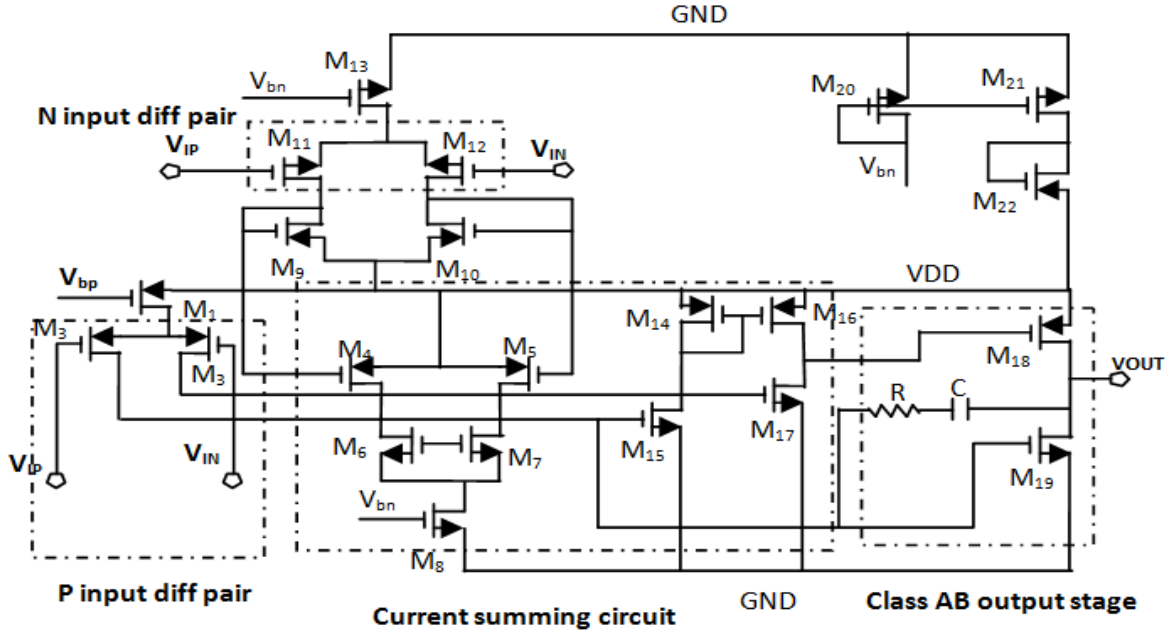

Fig 2: Two stage rail to rail error amplifier (EA)

The gain and swing of the amplifier must be more in order to reduce the aspect ratio requirement of the power MOS transistor. The gain of the first stage and second stage is given by equation (1) and equation (2) respectively. The total gain is the sum of these gains in dB i.e. in equation (3).

$$A_{v_1} = \frac{g_{m_1}}{g_{ds_1} + g_{ds_4}} \quad (1)$$

$$A_{v_2} = \frac{g_{m_6}}{g_{ds_6} + g_{ds_7}} \quad (2)$$

$$\text{Total Gain} = A_{v_1} + A_{v_2} \quad (3)$$

B. Power Mos Transistor.

Power MOSFET used is the PMOS with very high aspect ratio. Even NMOS can also be used but it is unfeasible for sub 1V operation. The size of the power MOSFET is based on the dropout voltage and the maximum load current required. The dropout voltage and maximum load current are related as given in equation (4). From this relation the power MOS aspect ratio is designed.

$$V_{dropout} = \sqrt{\frac{2I_{max}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p}} \quad (4)$$

C. Curvature Compensated Bgr.

The proposed piecewise corrected BGR is shown in Fig.3. It consists of consists of a conventional first-order BGR startup circuit, a conventional first-order BGR and the proposed curvature-corrected current generator. The first order BGR circuit generates a reference with slightly negative temperature coefficient as is given in Fig.4. The curvature-corrected current generator gives a piecewise nonlinear current given in equation (5) to correct the nonlinear temperature dependence to get lower negative TC as shown in Fig.4.

$$I_{NL} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \left(V_{SG-M_{12}} - |V_{THP}|\right)^2 (1 + \lambda V_{DS}) \quad (5)$$

$$V_{SG-M_{12}} = V_{DD} - \frac{R_5 V_T \ln(n)}{R_2} \quad (6)$$

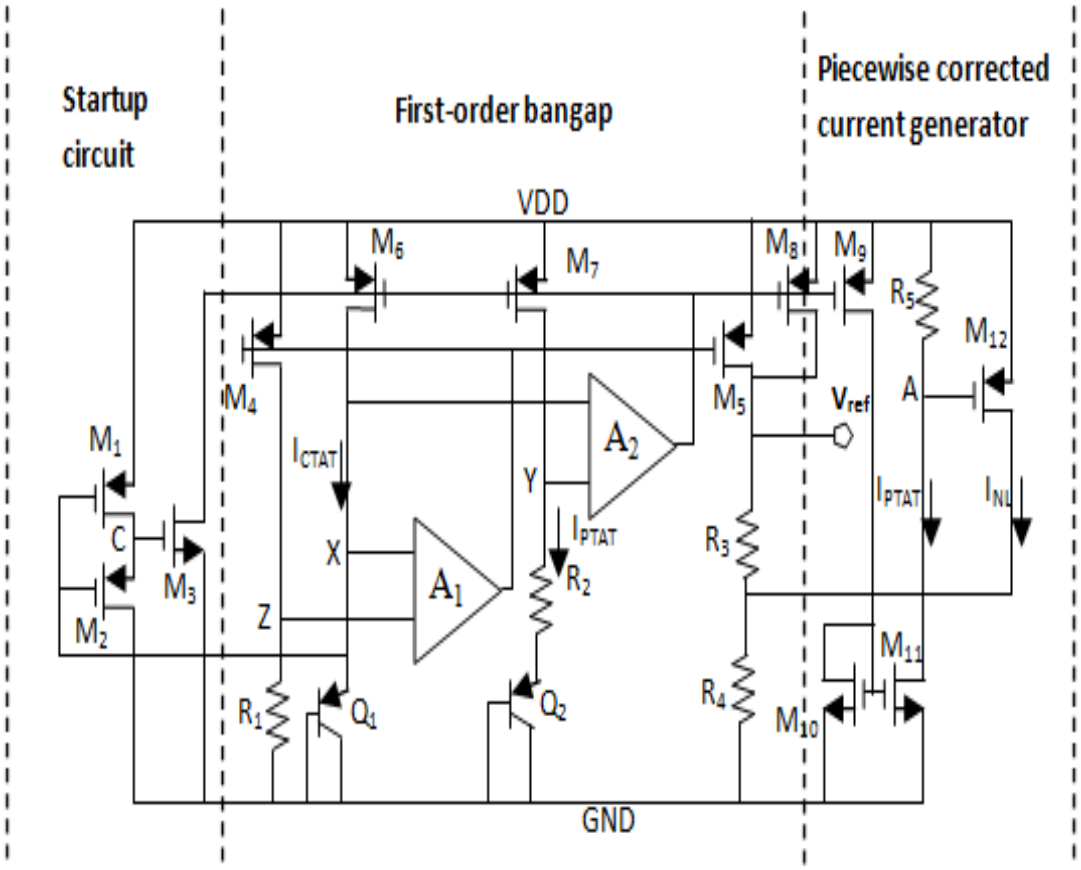

Fig 3: Piecewise curvature compensated BGR

Proposed architecture uses two NMOS differential input op-amps, one is used to generate PTAT and second op-amp is used to generate a CTAT.

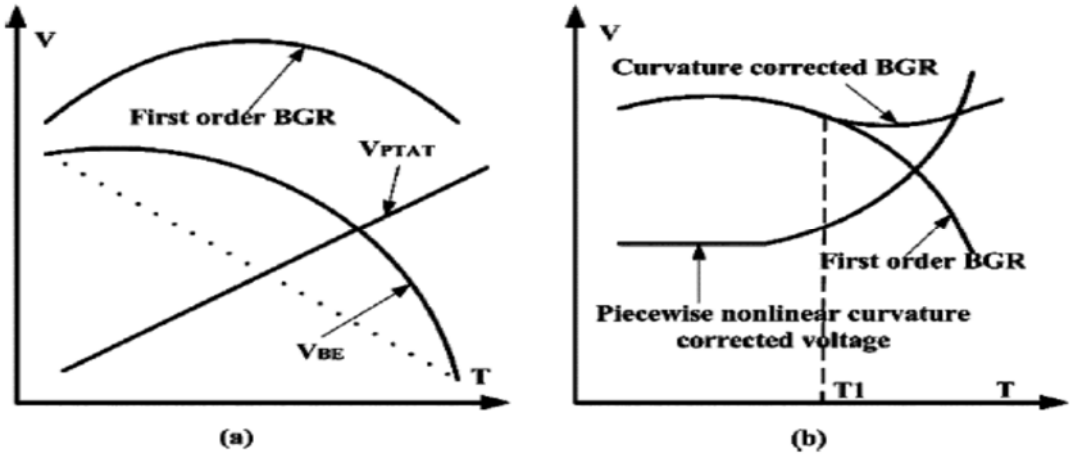

Fig 4. Reference curves for first order and curvature compensated BGR

Due to the positive TC of R_5/R_2, a PTAT voltage is generated at the gate-source voltage of transistor M_{12}. This voltage is used to overcome the negative TC and tries to move the reference curve upwards with respect to

temperature. The reference voltage generated by piecewise curvature compensated BGR is 0.5 V.

D. Feedback Network

The feedback network consists of two resistors R1 and R2. These resistors are designed depending on the regulated output voltage required and the reference voltage from bandgap reference circuit as given in equation (7).

$$V_{out} = \frac{(R_1+R_2)}{R_2} * (V_{ref}) \quad (7)$$

4. Implementation, Results & Analysis

The complete schematic circuit of the error amplifier is rigged up in virtuoso schematic editor and is as shown in Fig.5. It consists of NMOS and PMOS differential input stage.

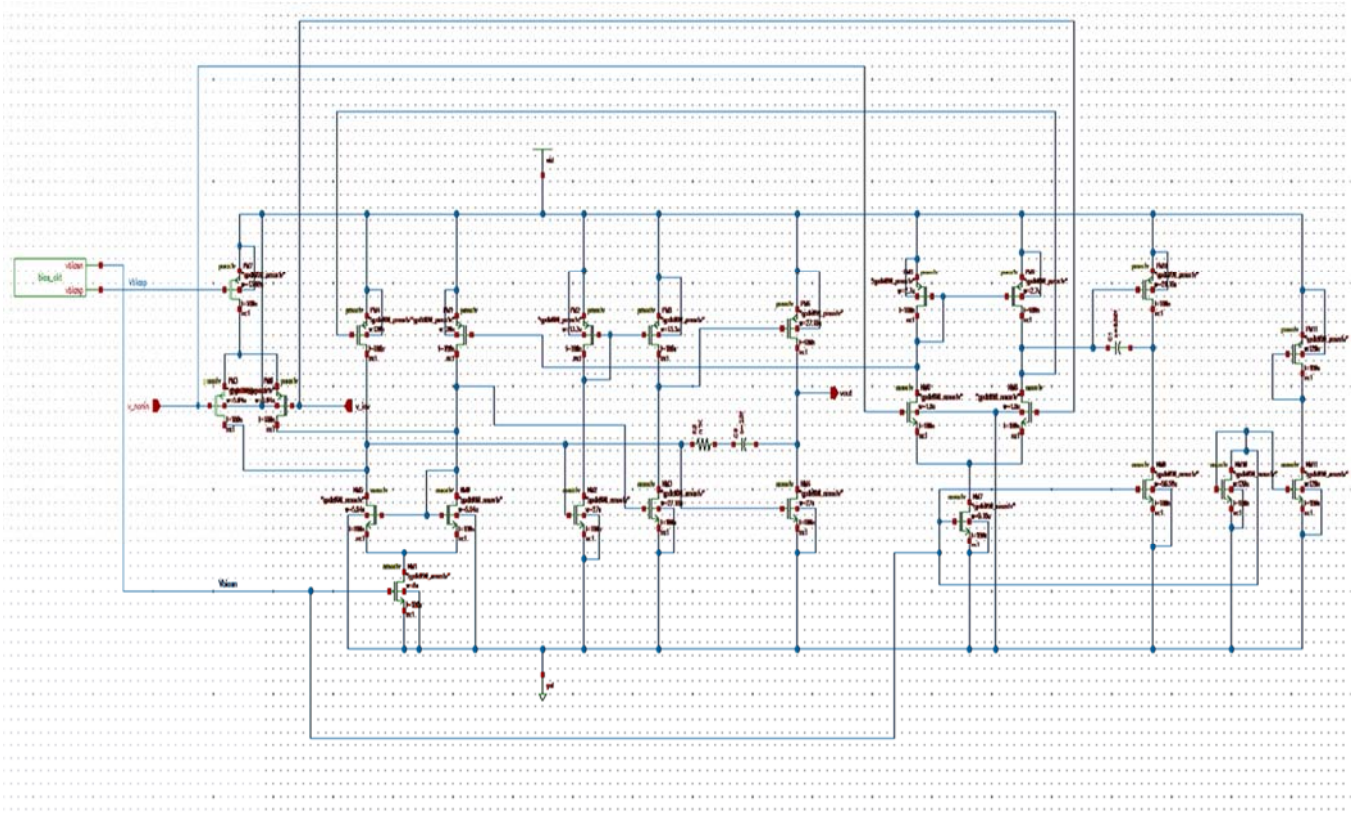

Fig 5: Two stage error amplifier (EA)

The gain of the EA obtained is 48.929dB and the gain plot is shown in Fig.6.

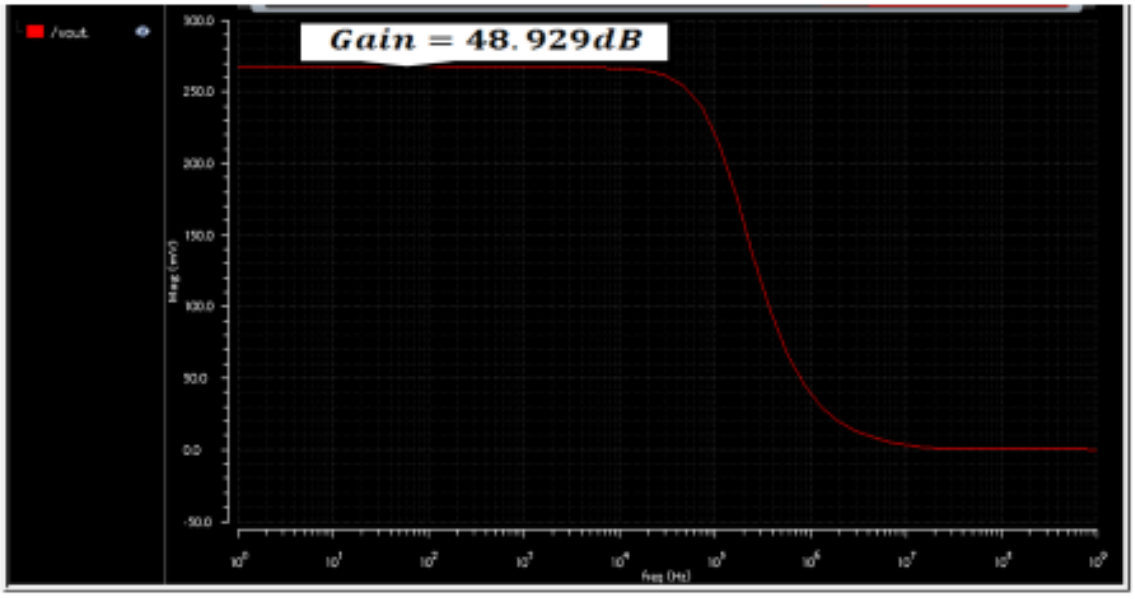

Fig 6: EA gain plot

The piecewise curvature corrected BGR is shown in Fig.7 and the output obtained with respect to the temperature is shown in Fig.8.

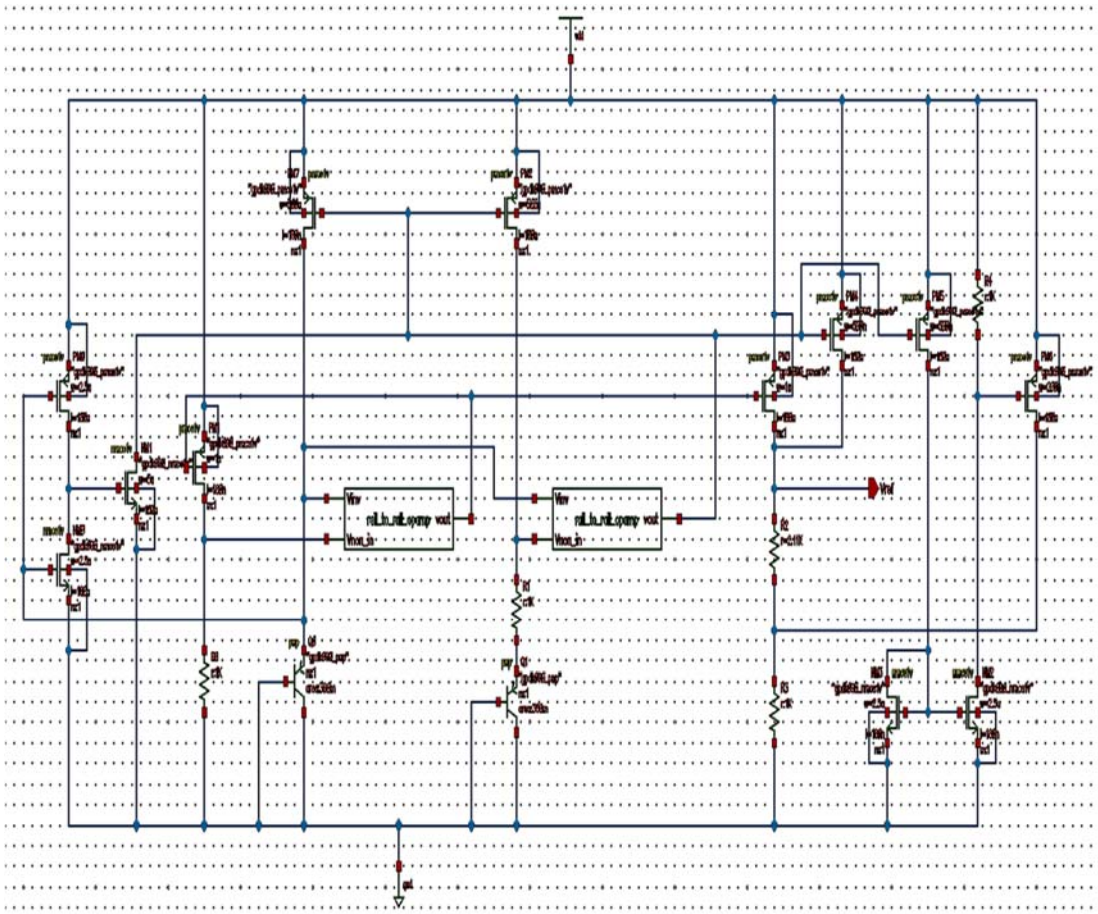

Fig 7: Piecewise curvature compensated BGR

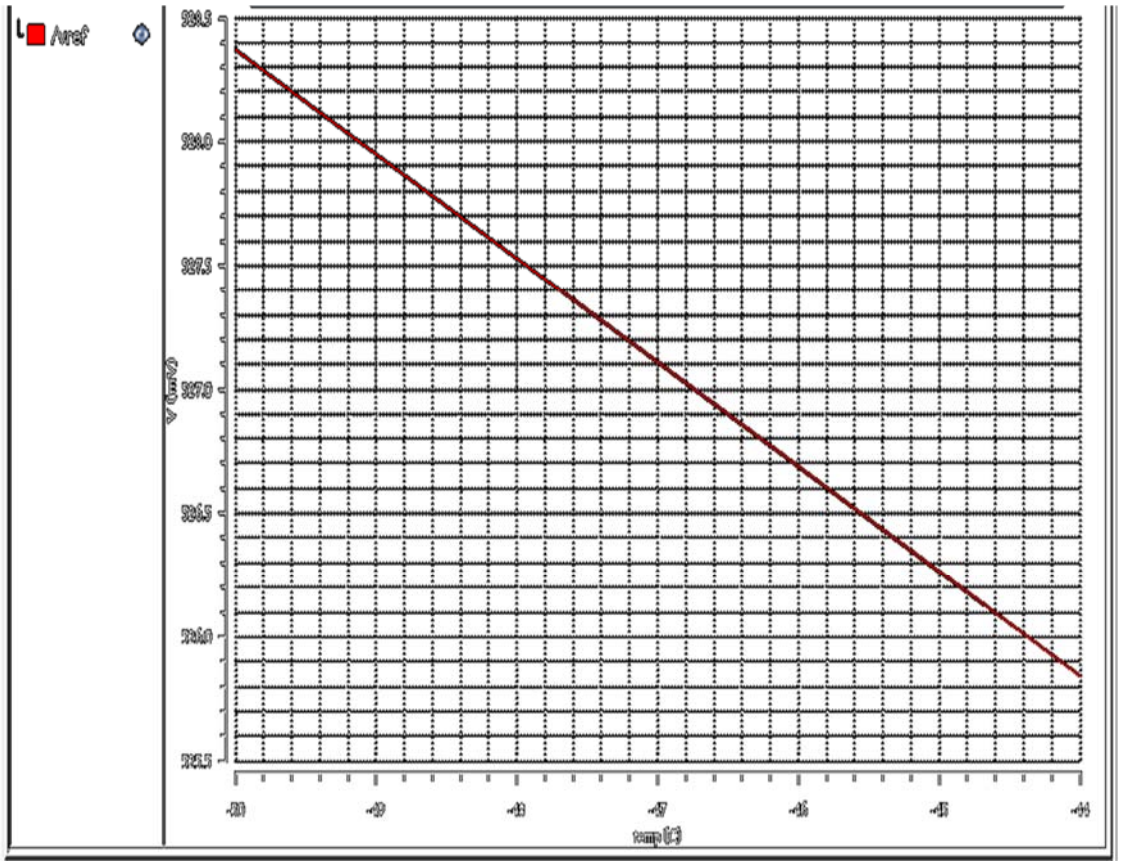

Fig 8: BGR output curve

The complete LDO regulator circuit is constructed in cadence virtuoso schematic editor and is shown in Fig.9.

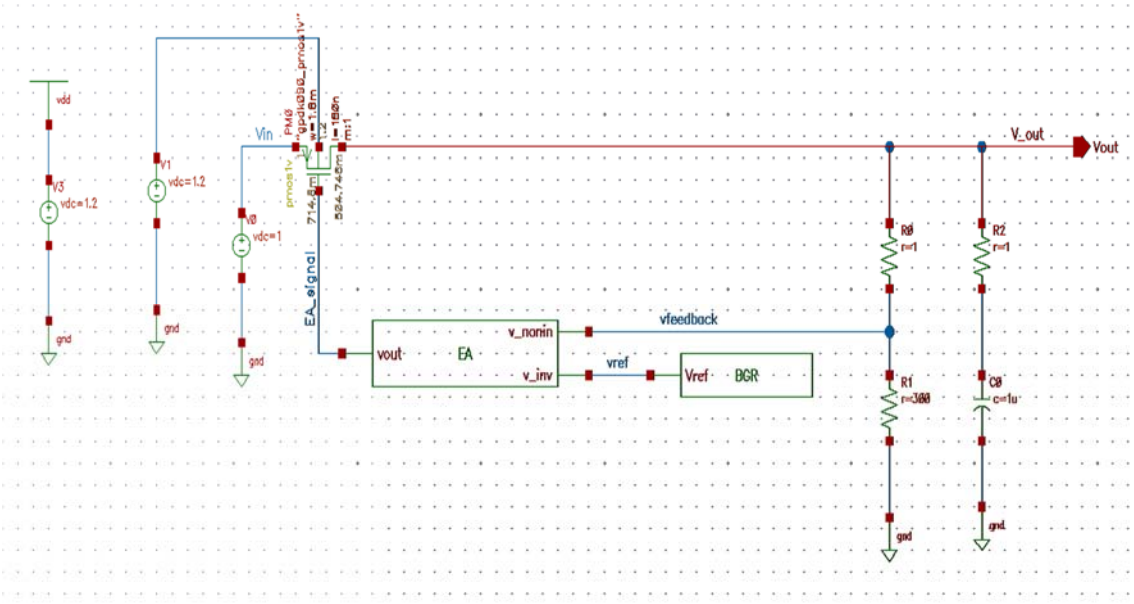

Fig 9: Complete LDO regulator circuit

The LDO regulator test circuit with load resistance R_L for load regulation is shown in Fig.10.

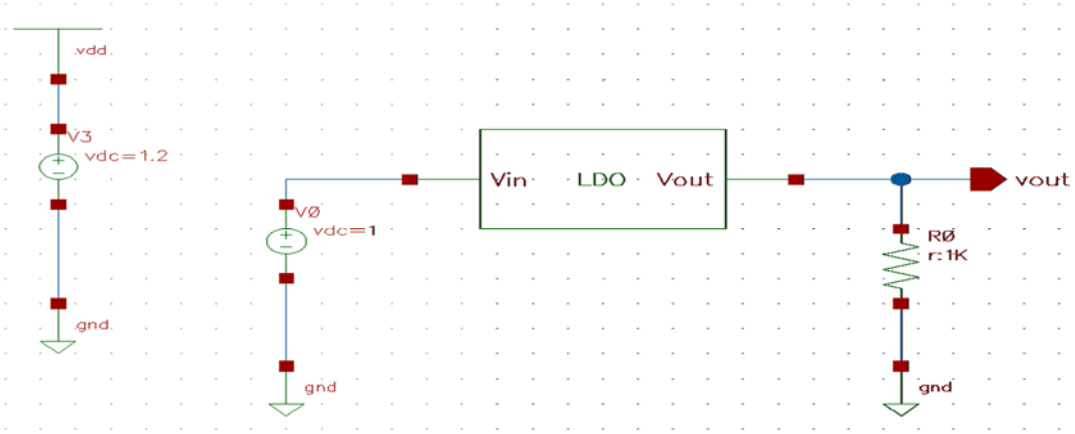

Fig.10. LDO regulator test circuit with R_L

This LDO can be tuned in the range from 0.5 V to 0.932V in increments of 50mV and 100mV. This can be done by changing the values of feedback resistors R1 and R2 .

Case (1): When LDO is tuned at a regulated output voltage of 500mV.

The LDO can be tuned to 500mV by using resistors R1 and R2 at the output side to 1Ω and 300Ω respectively. Fig.11. shows the outputs from internal blocks.

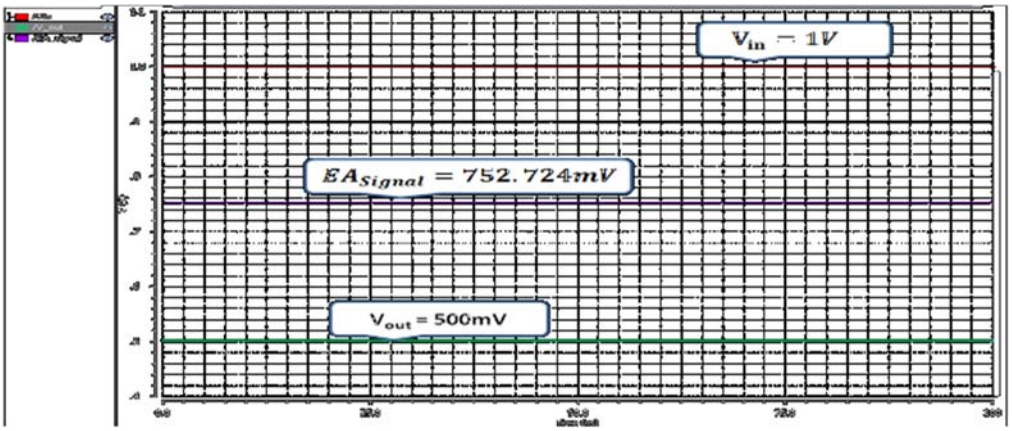

Fig.11. LDO outputs when it is tuned to 500mV

It can be seen from the above figure that the output from Error amplifier is 752.724mV in order to keep power MOSFET in saturation region so that the output will be a regulated voltage i.e. 500mV. The line regulation is plotted in Fig.12. The corresponding values of output versus input are tabulated as shown in the table 1.

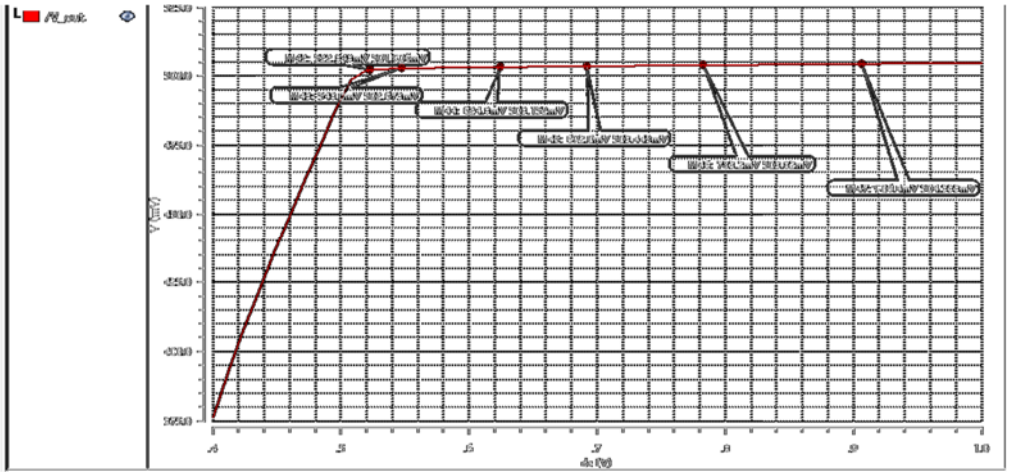

Fig 12: V_{out} vs. V_{in} at 500mV regulated voltage

Table 1: V_{in} and V_{out} at 500mV regulated voltage

Vin(mV)	Vout(mV)
522.848	501.906
548	502.67
624.8	503.152
692	503.443
692	503.82
783.2	503.906

Case (2): When LDO is tuned at regulated output voltage of 932mV.

The LDO can be tuned to 932mV by using resistors R1 and R2 at the output side to 258Ω and 300Ω respectively. Fig.13. shows the outputs from internal blocks when LDO tuned at 932mV. The line regulation is plotted in Fig.14. for regulated voltage of 932mV. The corresponding values of output versus input are tabulated as shown in the below table 2.

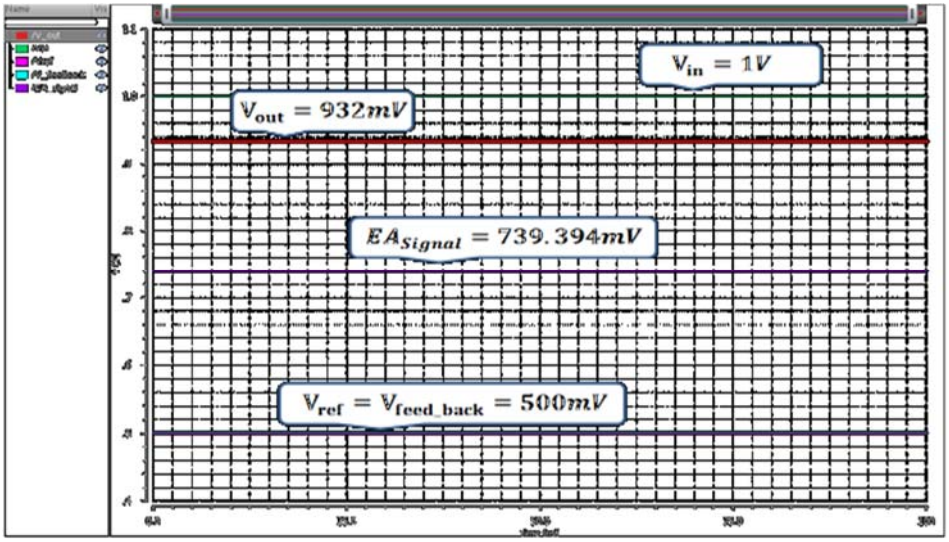

Fig 13: LDO outputs when it is tuned to 932mV

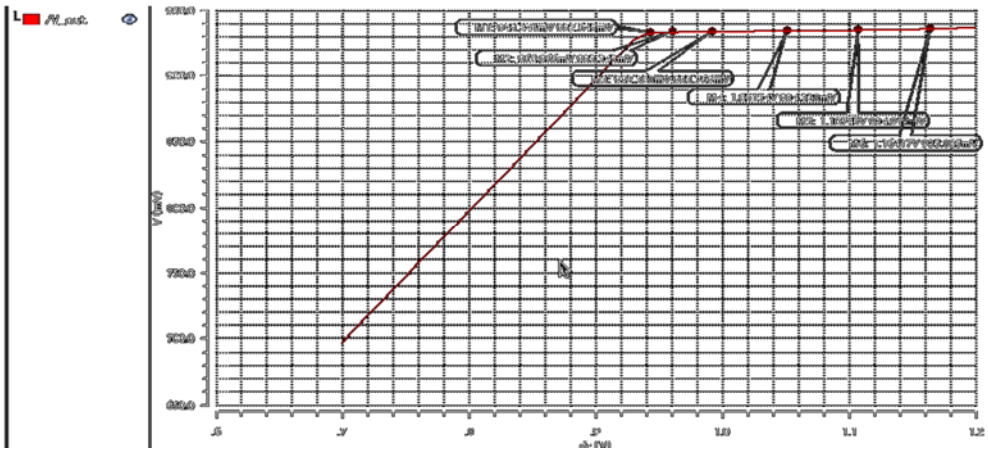

Fig 14: V_{out} vs. V_{in} at 932mV regulated voltage

Table 2: V_{in} and V_{out} at 932mV regulated voltage

Vin(mV)	Vout(mV)
943.241	932.643
960.966	933.343
992.308	933.769
1.0514	934.326
1.0745	934.915
1.16417	935.805

Variation of output voltage with respect to load resistor (load regulation) is shown in Fig.15.

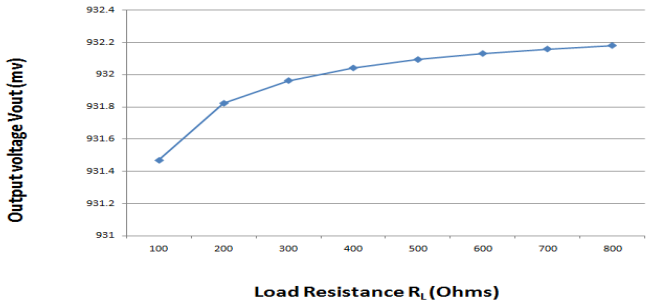

Fig 15: Load Regulation at 932mV output voltage

It can be seen from the above graph that the variation of output voltage is very less with respect to the load current i.e. load resistor R_L which is a good characteristic of LDO. Finally all the parameters of LDO regulator are tabulated in the table 3 and in the same table all the parameters of this work are compared with the recent previous work [1]. In this work the quiescent current and dropout voltage are decreased to a very less value.

The layout of the complete LDO circuit is as shown in figure 16.

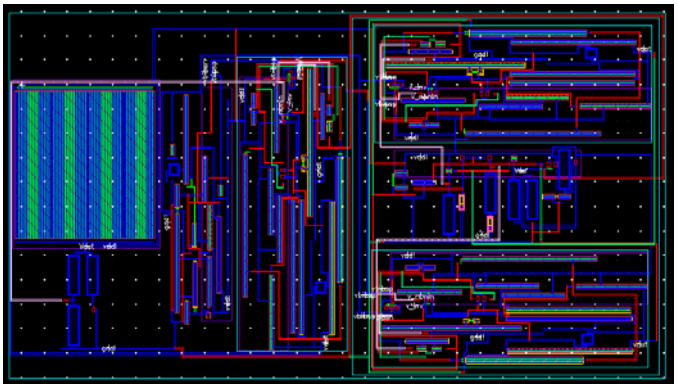

Fig 16: Layout of complete LDO

Table 3: Comparison of LDO Parameters

Parameters	[1]	This work
Technology	90nm	90nm
Vin	1V	1V
LDO Tuning Range	0.5 – 0.85	0.5 – 0.932
Dropout Voltage	150mV	68mV
Max Load current, Imax	100mA	1mA
Quiescent Current, I_Q	60µA	0.4µA
Current Efficiency	99.94%	99.99%
Efficiency of LDO	84.94%	93.19%
Line Regulation	-	7.41mV/V
Load Regulation	0.28mV/mA @ Vout =0.85V	0.11mV/mA @ Vout = 0.932V
Area	0.0041mm^2	0.018 mm^2

5. Conclusion

The paper describes a LDO which is having so many advantages over recent works. It is having high efficiency, very less dropout voltage and very less quiescent current which are the characteristics of good LDO. The LDO output is invariable to temperature since reference voltage for regulator is derived from BGR circuit. The LDO can provide stable voltages in the range from 0.5V to 0.932V and this range of voltages can be used as stabilized source voltages for devices working in sub 1 V operation.

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