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Designing & Analysis of Advanced Turbo Encoder and Decoder

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Abstract
Turbo coding is an advanced error correcting technique widely used in communication field to achieve reliable information transfer over bandwidth in presence of data corrupting noise. Viterbi algorithm is a maximum-likelihood algorithm for decoding of convolutional codes. This algorithm has good correcting capability & perform well even in presence of very noisy channels. Turbo encoders & turbo decoders are the key elements in today`s communication system so as to achieve the best data reception with fewest possible errors. In this paper, an efficient VLSI architecture for advanced turbo encoder & turbo decoder using the convolutional interleaver has been designed & implemented for code rate of 1/3. Interleaver is known to be a main obstacle for decoder implementation introducing latency.

Keywords: Convolutional interleaver, Turbo encoder, Turbo decoder, Viterbi Algorithm etc.

1. Introduction
In Today's digital wireless communications world, error detection and correction for transmission of data are most important issue for communication channels. By detecting and correcting the errors, the capacity of the source data transmission improves. Forward error correction (FEC) is an advanced technique for error control during data transmission, whereby redundant information is added to the original data, which allows the receiver to detect and correct errors without the requirement to resend the data. The main advantage of FEC is to avoid the retransmission at the cost of higher bandwidth requirements and hence is employed in the situations where retransmission is relatively costly or unworkable. In information theory, turbo codes are a class of high-performance forward error correction (FEC) codes, which were the first practical codes to closely approach the channel capacity, a theoretical maximum for the code rate at which consistent communication is still possible given a specific noise level. Turbo codes are finding use in (deep space) satellite communications and other applications where designers seek to achieve reliable information transfer over bandwidth- or latency-controlled communication links in the presence of data-corrupting noise. Turbo codes can be implemented by designing the Turbo Encoder and Decoder by viterbi algorithm. The Viterbi algorithm is a best decoding technique with minimum possibility of errors.
HEMA.S. *et al.* [5] presented a field-programmable gate array implementation of viterbi decoder with constraint length of 11 with a code rate of 1/3. It shows that the larger the constraint length used in a convolutional encoding process, the more powerful the code produced. Also, In 2013, Pooran Singh and Santosh Kr. Vishvakarma [6] worked on, "RTL level implementation of High Speed-Low power viterbi encoder and Decoder", IEEE. They worked based on making of fast viterbi encoder- decoder with low power consumption.

Turbo Code System
The Turbo codes has outstanding bit error rate (BER) performance at much lower power levels. Implementation of Turbo codes consists in designing the Turbo Encoder and Decoder. Turbo coding technique consists of a parallel concatenation of two binary convolution codes, decoded by Viterbi Decoding System. Thus, two systematic convolution encoders that are usually known as recursive systematic convolution (RSC) encoders are concatenated in parallel. In this parallel concatenation, a random interleaver plays a very vital role by rearranging bits in certain predefined order. The first encoder encodes an original copy of

data, whereas the second encoder encodes an interleaved form of data. The outputs of two RSC encoders and interleaver are added together to get a bit stream of 3 times the original bit stream, means for single input bit, it produces 3 bits. It will be then transmitted to the channel. This coding scheme is decoded by means of Viterbi Decoder system.

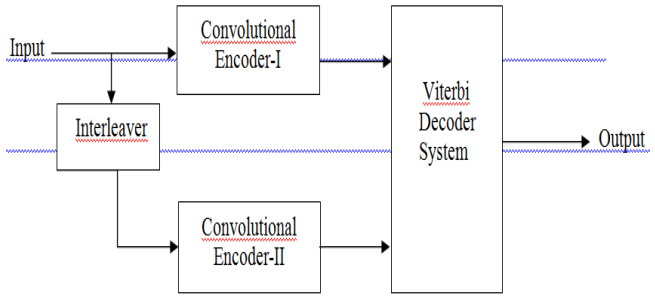

Fig 1: Block Diagram of Turbo Code System

Turbo Encoder

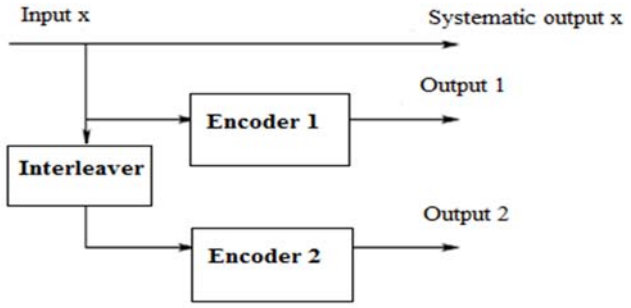

Fig 2: Block diagram of Turbo encoder

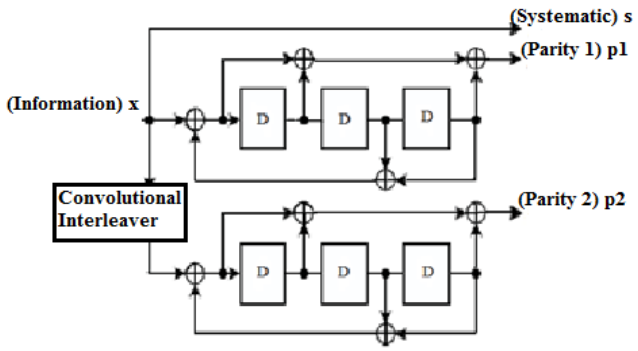

Fig 3: Structure of Turbo encoder

Two systematic convolution encoders are arranged in parallel concatenation, so that each input element is encoded twice, but the input to the second encoder passes first through a random interleaver. The systematic encoders have code rate R= 1/3. In order to improve the rate, another useful technique normally included in a turbo coding scheme is puncturing of the convolutional encoder outputs. It encodes a N-bit information data block to a code word with 3N+12 data bits, where these 12 tail bits are used for trellis termination. While starting the encoding of the bits, the initial value of the shift registers of the encoders shall be all zeros always.

Interleaver

An interleaver is a hardware device that takes symbols from a fixed alphabet as the input and produces the identical symbols at the output in the different temporal order in order to minimize the effect of burst errors introduced in transmission.

A convolutional interleaver consists of N rows of shift registers having different delay for each row. In this, each successive row has a delay which is J symbols duration higher than the previous row as shown in Fig 4. The code word symbol from the encoder is fed with one code symbol to each row. With each new code word symbol, the commutator switches to a new register and the new code symbol is shifted out to the channel. The convolutional deinterleaver performs the inverse operation of the interleaver.

As per the fig.5 of 8-bit convolutional interleaver, the code word symbols (Din) received in serial form from an encoder is converted into a 8 bit parallel code word by a Serial Input Parallel Output (SIPO) register. The next buffer unit transfer a word to the delay unit after every 8 clock cycles. The delay unit has eight rows. Each code symbols of the 8 bit code word is thus applied to the respective row of the delay unit. The code word gets twisted as it progresses through the delay unit. This twisted form of code word is then applied to the input of an 8:1 multiplexer (MUX) which converts it into stream of serial data (Dout). The interleaver circuit requires a clock signal to drive the SIPO register, a clock circuit and a three bit counter.

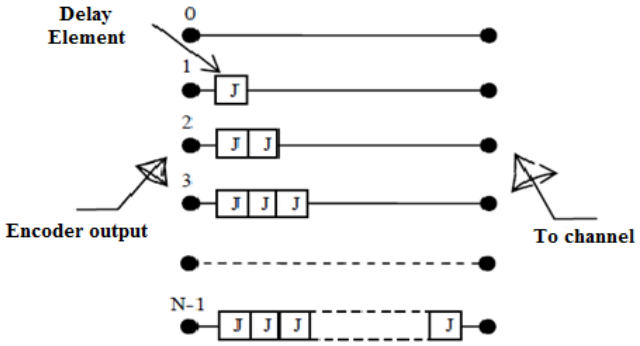

Fig 4: Convolutional Interleaver

The structure of the deinterleaver is exactly similar to Fig.5. The twisted form of code words from the output of the interleaver is applied as input to the deinterleaver block along with clock as synchronization signal. Thus, the twisted code word is converted into its original form at the output of the deinterleaver block.

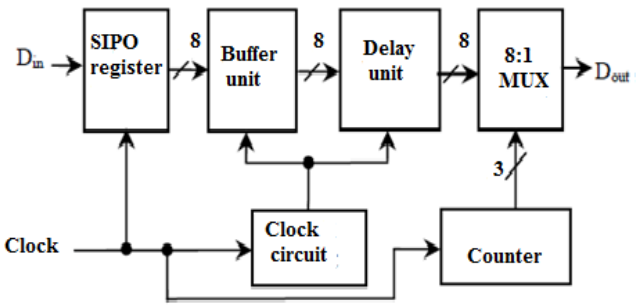

Fig 5: Block diagram of proposed 8-bit convolutional interleaver

Turbo Decoder

Viterbi decoder is mainly employed for encoding the convolutional data as it can overcome number of errors received at the input data due to channel noise. The Viterbi decoding algorithm is a state of the art algorithm used to decode convolutional binary code used in communication standards. It is the optimum decoding technique with minimum possibility of error. A Viterbi decoder typically consists of three building blocks, as shown in Fig.6:

- **Branch Metric Unit (BMU)**

This unit calculates the likelihood for the possible transitions in a trellis. For each transition the block computes the branch metric or a hamming distance. Hamming distance is the distance calculated between the expected signal and the received signal. This unit finds the reliable way to encode the data.

- **Path Metric Unit(PMU)**

The path metric is calculated by finding the minimum cost of arriving signal into a specific state. A previous time instant of state metric is added with the branch metric and selected the smaller one for each state. In this manner the path metric unit works.

- **Add-Compare-Select Units (ACSUs)**

This discard suboptimal trellis branches based on current branch metrics and previously accumulated state metrics. Add and compare select unit (ACSU) consists of two storage unit as state metric storage unit and survivor path storage unit. The state metric storage unit stores the partial path metric. The survivor path storage unit thus stores the selected path.

- **Survivor Path Memory Unit (SMU)**

It works upon the decisions from the ACSUs to produce the decoded bits along the reconstructed state sequence through the trellis.

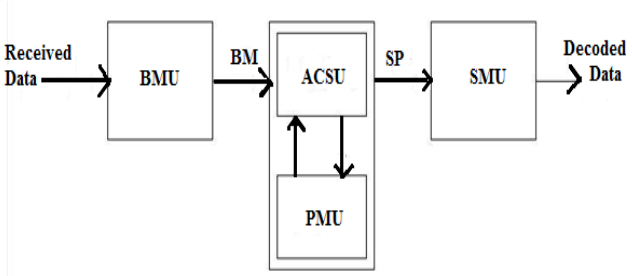

Fig 6: Block diagram of Viterbi decoder

2. Performance Analysis

VHDL model of complete turbo encoder & decoder has been developed. The Turbo encoder composed of total three blocks out of this, two blocks are convolutional encoder and one is convolutional interleaver. This design is synthesized & simulated using Xilinx 9.2 ISE.

Following fig 7 & fig. 8. shows the complete output waveform of turbo encoder & testbench waveform of complete VHDL model.

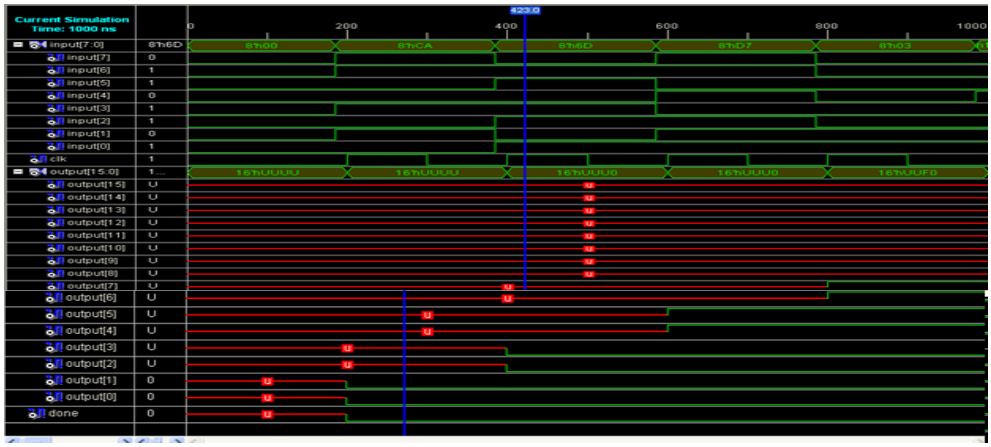

Fig 7: Output waveform of Turbo Encoder

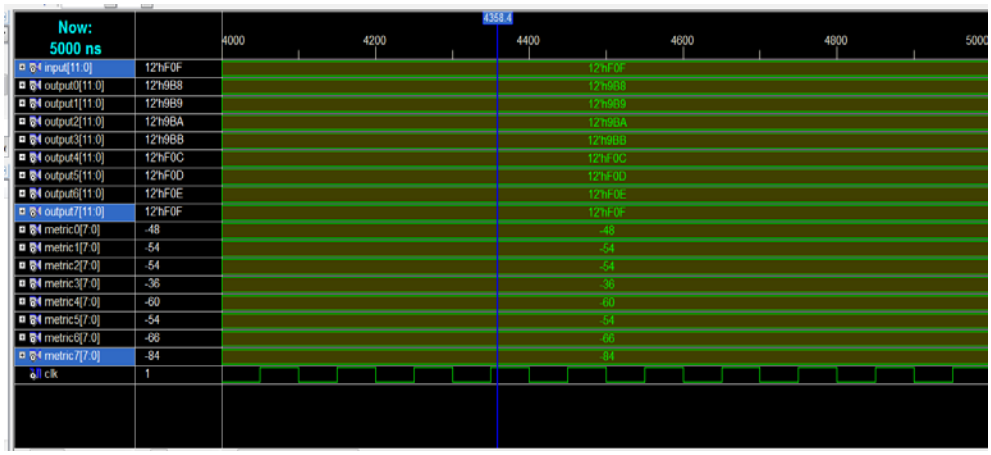

Fig 8: Testbench Waveform for VHDL Model

3. Conclusion

The aim of this paper is **t**o check & verify the functionality of Turbo encoder & Turbo decoder using Viterbi algorithm on Xilinx. Thus, an efficient architecture for turbo encoder & turbo decoder has been implemented using VHDL. These configurations give better performance and also has the lower computational complexity.

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