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Implementation of fault tolerant soft processor on FPGA

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Abstract
This paper presents design of fault tolerant soft processor and implementation of it on FPGAs. Due to configurability feature and increasingly complex architecture of Field Programmable Gate Arrays (FPGAs) have brought advantages to many applications such as avionics applications and safety critical aerospace. These features of FPGAs allows in system reconfiguration after launch. To enhance FPGAs functionality embedded processors, either soft cores using reconfiguration logic of FPGA or built in hard cores on Xilinx FPGAs, have been up taken in many applications due to close compatibility with high level applications and their flexibility. The most commercial FPGAs suffer from radiation induced faults, which are provoked by high energy particles in space. To harden the fault tolerance of soft processor technique used is Error-correcting code technique. This technique is used especially for memories of soft processors. Error-correcting code technique is demonstrated in implementation of a fault tolerant soft processor on Xilinx FPGAs. In additional we used Look Ahead technique to synchronize Error-correcting code-protected Block Read Access Memory (ECC BRAM) with the soft processor. Without halting the processor, the resulting fault tolerant soft processor has benefit to self recover the memory in presence of Single Error Upsets.

Keywords: Fault tolerance, SEU (Single Error Upset), Field Programmable Gate Array (FPGA).

Introduction
In mission critical applications FPGAs are attractive. As architecture of FPGA is complex and has configurability feature, which have brought advantages to many applications such as avionics applications and safety critical aerospace. In Xilinxs FPGA two types of processors are included. On FPGA hardcore processors are hard wired and their numbers are limited. Whereas soft core processors numbers depend on device size and are reconfigurable. Soft core processors has increased uptake in many applications because of compatibility and flexibility with high level applications. SRAM based technologies are affected by noise and these produces soft errors. Many of commercial FPGAs, which are SRAM based FPGAs suffer from higher radiation induced faults e.g. Single-Error Upsets (SEUs). In space due to high energy particles these faults are provoked. Due to Single-Error Upsets (SEUs) faults, memory cells of FPGAs are hardened than traditional SRAMs to robust. Memory cells of FPGAs are hardened for fault-critical applications example in space [1].
Memory module contains more data which are manufactured with small cells so they are still unprotected. Memory module is used to store program and data memory by most FPGA soft processors. This memory module when used in safety critical applications requires more attention. For memory module built-in Error Correcting Code (ECC) circuitry is developed by Xilinx [2]. ECC is an effective solution to detect and correct single bit error. Fault tolerant versions of soft processors needs to be synchronized with ECC mechanism. The complete process of error-correction runs without any latencies or noticeable delays. And ECC does not require any specific hardware. This is demonstrated in design and implementation of a fault tolerant soft processor.

Background Study
Previously, LEON-3FT was proposed by European Space Agency, ESA, in 1997. LEON-3FT is open source Fault Tolerant version [3]. LEON project was studied and developed for a high-performance processor, which is used in European space projects. LEON is a 32-bit CPU microprocessor core, based on the RISC architecture and instruction set. The core is suitable particularly for system-on chip (SOC) designs and highly configurable. LEON 3FT

is a Fault-Tolerant (FT) version, designed for operation in radiation-prone environments and harsh. LEON detects and corrects errors which are caused by SEU's in processing unit. LEON consumes more resources.

Next technology was radiation hardened processor [4]. These processors are built with special design libraries and fabrication processes. These designs and processes are more resilient to high energy radiation. Although this technique is tolerant to radiation, radiation hardened processors are larger, slower, consume more power and costly.

A large amount of research and testing has identified techniques for mitigating the effects of radiation induced upsets in electronics, specifically in FPGA designs. Most mitigation approaches use either a monitoring and scrubbing unit an internal monitor or external to FPGA. If scrubber is external, it is typically implemented on separate RadHard processor such as FPGA, ASIC or PLD. External scrubbing typically performs constant rewrites memory values whether or not upsets have occurred in memory cells. This scrubbing increases cost, power consumption, and board area and design complexity. And decreases design flow flexibility. If the scrubber is internal, it may use hardware modules to calculate Cyclic Redundancy Check (CRC) values of frames of configuration bit stream and compare them to known CRC value for each frame [5]. But CRC modules are susceptible to radiation induced errors.

Triple Modular Redundancy (TMR) is the classic and most commonly used error mitigation technique for SRAM based FPGAs. TMR provides fault tolerance by triplicating a user design and instantiating a voter to vote to outputs of three modules. It triplicates functioning modules and if any one module fails majority voter is used. Implementing TMR in a design can incur power and area costs of up to three times more than non triplicated design would require [6].

Fault Tolerence

Fault tolerance (FT) is the ability of a system that enables it to continue its operation even in presence of faults. As failure of system reduces maintenance cost reduces of Fault tolerant design [7]. Fault tolerant is an important feature for many operating applications, from automotive to space applications. It is applicable in life critical applications. It also provides improvement in system availability.

There are two ways to express fault tolerant i.e. availability and reliability. Availability is expresses fraction of time system is operational. System with high availability may fail it should noted. High availability is important in many applications such as telephone and airline reservation switching where every minute of failure leads to revenue loss.

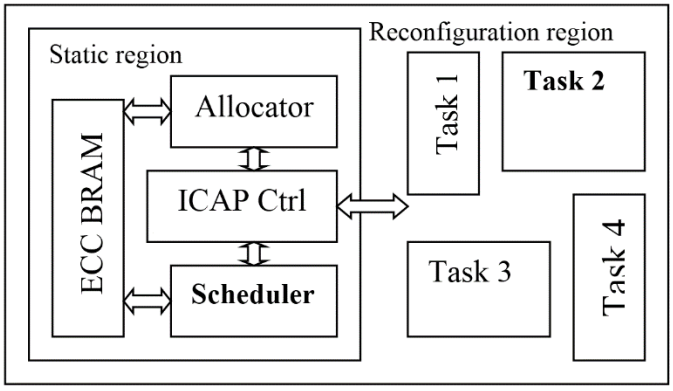

Fig 1: Overall system architecture

Reliability is the likelihood that a system will remain operational despite of failures for the duration of a mission. In critical applications high reliability is most important e.g. industrial control or space shuttle. In such an applications failure could mean loss of life.

Overall System Architecture

In FPGA devices, during runtime in configuration memory faulty bits can be reconfigured [8]. This is called dynamic reconfiguration, which can bring practical solution.

FPGA chip is divided into two regions in overall system architecture: reconfigurable region and static region (Fig 1). In static region main system is located. And in reconfiguration region hardware tasks can be in/out swapped. In static region, to protect system ECC technique is used. And in reconfiguration region scrubbing or task relocating away from damaged resources is used for fault tolerance.

In static region, three kernel processors exist i.e. task scheduler, task allocator and ICAP controller. Task scheduler schedules hardware task. Task allocator allocates the hardware task. ICAP (internal configuration access port) configures hardware task in real time [9, 10].

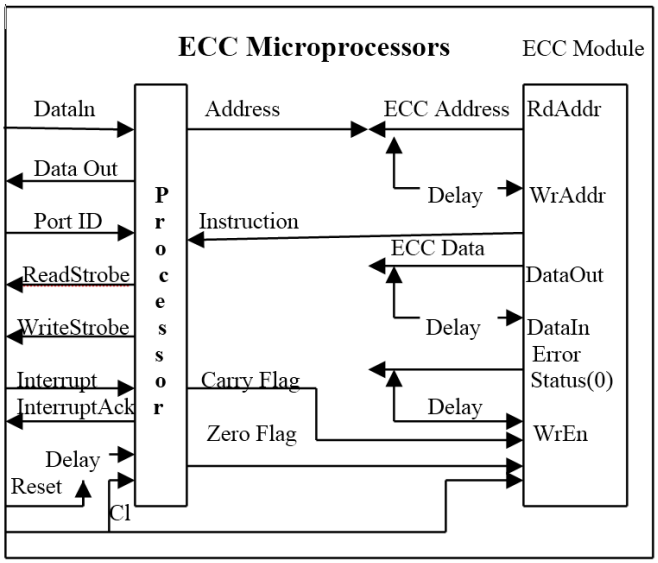

Fig 2: ECC Microprocessor

Ecc Microprocessor

Error Correcting Code microprocessor consists of two main blocks: processor, EPA and Error Correcting Code BRAM figure 2.

Processor

32 bit Xilinx soft core processor is used. Processor is completely described in a hardware description language (HDL) that is in verilog. Implementation of program memory is in BRAM.

Error Correcting Code BRAM

Error correction code is added to BRAM blocks. Using Error correction code detection and correction of single error is possible.

Rtl View and Simulation

RTL view

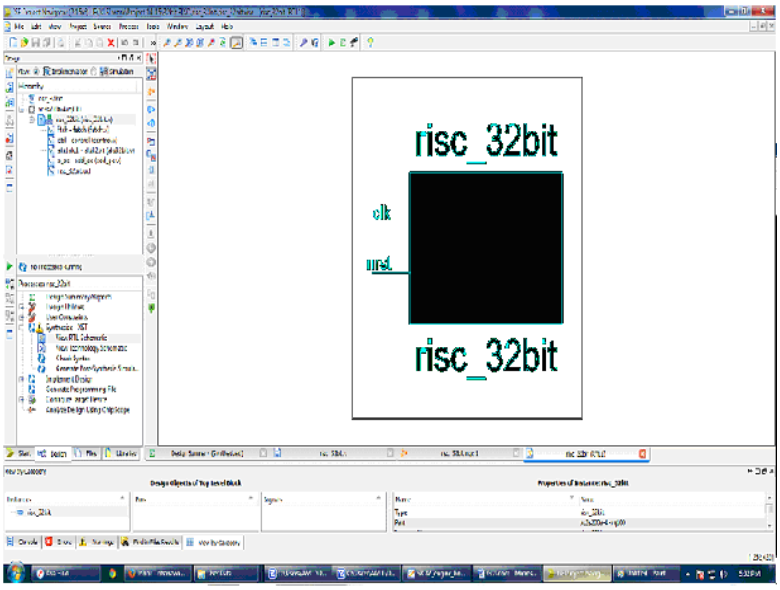

Fig 3: RTL view of 32 bit processor

Figure 3 shows the RTL view of 32 bit Xillinx soft core processor.

Simulation

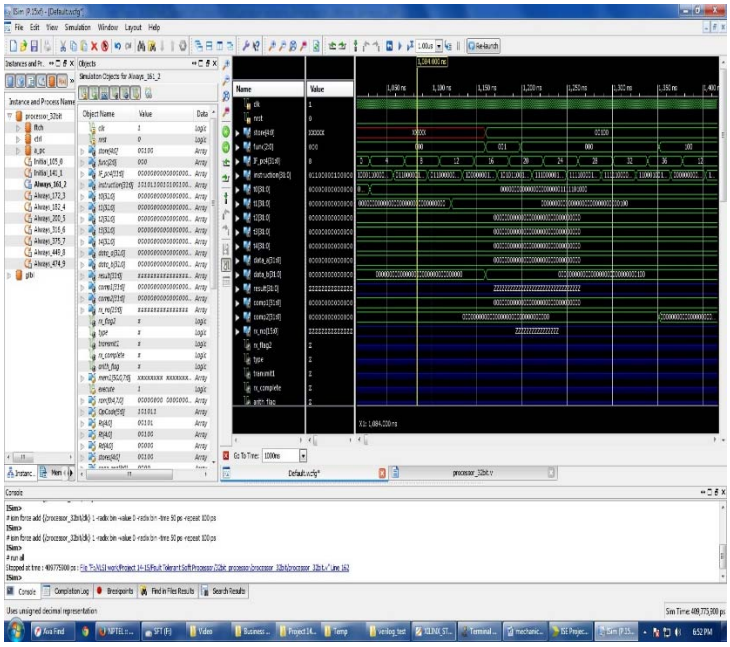

Fig 4: Simulation result of 32 bit processor

The memory is automatically corrected. Single Error Upset is detected and corrected by error correcting code.

Conclusion

In this paper, we implemented fault tolerant soft processor on FPGA, using Error correcting code program memory. 32 bit Xilinx soft core processor is designed and implemented on FPGA. Error Correcting Code is used with soft core processor for detecting and correcting single error upsets. This architecture works without affecting execution of processor.

These can be further improvised to porting with other FPGA soft processors.

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