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A Survey on factors causing power consumption and their reduction techniques of embedded Processors

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Abstract
An embedded system is a computer system with a dedicated function within a larger mechanical or electrical system with a real time computing constraints. 98% of all microprocessor being manufactured are used in application domains such as communication, multimedia, networking. The life time of system depend on battery life that is determined by power consumption of entire system. We must explore the sources of energy consumption and basic techniques to reduce power consumption of the portable devices that uses battery power. This paper gives detailed study on factors causing power consumption, minimizing them by presenting the reduction techniques and technologies available. In this paper, first section deals with necessity of embedded processor with low power. Second section explains the factors causing power consumption. The design technique involved in system architecture, functionality, operating system and entire network plays a vital role in achieving efficient energy. Third section gives reduction techniques to increase the performance of the embedded processor.

Keywords: Embedded, Constraints, Technology, Performance

1. Introduction
An embedded processor is a microprocessor that is used in an embedded system. These processors are usually smaller, use a surface mount form factor and consume less power. Embedded processors are divided into two types: microprocessors and microcontrollers. There are different kinds of programmable embedded processors categorized by clock frequency, RAM size, data bus width, packaging type and I/O voltage. Embedded processor can be found in portable devices like digital watches, PDAs, digital cameras, GPS units and MP3 players. They can also be found in larger systems such as traffic light, systems controlling power plants, and factory controllers. Embedded processor are widely used for telecommunication and household appliances. All portable embedded system require real time processing capabilities and demand high throughput (efficiency). Design of an embedded processor or system to satisfy the consumer need has given rise to fabrication of integrated logic circuits inside the processor with increase in number of transistors and the count has crossed over 2.5 billion transistors on single chip. This increase in integration levels decreases the battery life so much effort has to be put in conserving the power at these levels. Portable devices consists of low power component and sub Systems that includes low power displays, lower power consuming CPUs, trans receivers etc... these low level circuits and logic technologies establishes improvement in energy efficiency but they do not hold on promise for longer battery life. General purpose that are programmable are not used as low power consuming devices instead SOC (system on chip), embedded processor core with accelerator, IP cores are used. Power is becoming a major treat to microprocessor. INTEL has cancelled the next generation TEJAS PENTIUM IV chips due power consumption issues. So power management plays a vital role in sophisticated and intensive applications.

The below block diagram gives the details of embedded systems:

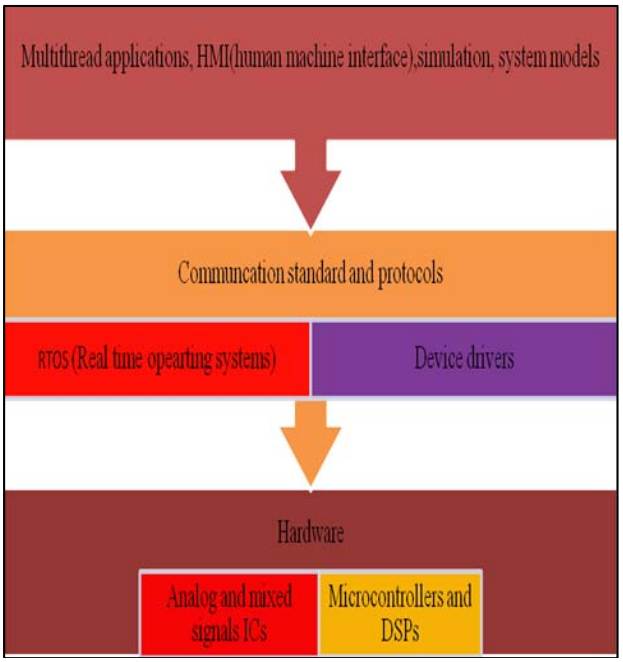

Fig a: Block diagram embedded systems

2. Low Power Necessity in Embedded Processors

At present, with the growing technologies there is a steady and increasing requirement of low power electrical devices. Before supporting a low power design, many significant factors are to be viewed which includes, QOS (quality of service), throughput, cost, reliability, temporary and functional requirement, performance, etc...

At past, the thirst of low power consumption was efficient to meet the requirement. But, nowadays, the demand for power consumption is increasing. The count of transistors increasing exponentially every year is supported by Moore's law which defines number of transistor doubles every 18 months. Increased performance and automation systems rapidly increases electrical load, which increases the power consumption. Therefore, a compact, less weight and robust design is urged for future applications. There are some typical characteristics that give the necessity of embedded in real time application.

- **Single function**

Unlike software packages such as word processor, spreadsheet, web browser or a database in a library. An embedded system executes only one program at a time.

- **Interact with real world directly**

Embedded systems are directly connected to real world environment via sensors and interfacing modules. Users can directly change the parameters whenever needed.

- **Works under tight constraints**

Embedded systems have limited resources in terms of memory, processing power and peripherals to interact with other systems. Power constraint is also major factor such that many devices have to run using small sized batteries for many years without any falter.

- **Mostly built as the reactive mechanism**

Reactive mechanism means such that the embedded system is designed for specific applications, their functioning is triggered by external response or feedback.

Above mentioned characteristics differentiate embedded systems from a general purpose computer or software and the need of embedded systems.

3. Factors Causing Power Consumption in Processor

The major of power consumption are transistor size, clock speed, switching capacitance, register file size, program execution time, insertion of wait states and cache miss. This section briefly explains of these topics.

(1) Transistor size

Inside the processor it is made up of the many MOSFET in a configuration we call as the CMOS circuit. The slowest path in the chip is said to be critical path that is often related with size of the transistor. Bigger the transistor longer is the critical path and slower is the clock rate. If you run the clock faster than the critical path the chip may malfunction due to some certain violations. A transitory size depends on channel (n channel, p channel) dimension, do pants, MOS process. As the transistor size gets smaller, no of transistor count rises in recent times but it leads to more leakage current that has critically major factor for the power consumption.

(2) Clock speed

Transistor density does not directly affect clock speed or clock rate. In CMOS circuit, if you change the value of gate of MOSFET you are just charging or discharging a capacitor. The CMOS will look as if like a capacitor model from gate. So we need to increase voltage up to threshold level since more transistor are used thus more power is consumed. Faster clock speed or high clock rate is essential in switching thus power consumption is more to high clock rate. Smaller processor possibly has high clock speed drive more transistor count in them. To fasten the logic level transitions over no of transistor in smaller processor we need to increase the clock rate that consumes more power for each transition.

(3) Cache misses

Cache is a smaller, faster memory which stores the copies of the data from frequently used main memory locations. Therefore, all the dates cannot be stored in cache which leads to "cache miss". This leads to increased instruction which further leads to additional clock cycles are wasted to find data and delay is provoked. This delay consumes more power that is one of the sources of power consumption.

(4) Switching capacitance

Already discussed CMOS circuit will be viewed as capacitor model there are two factors to determine the power consumption.

- Static power consumption: CMOS have very low static power consumption that result in leakage current. The CMOS output in the processor drives other CMOS logic gates, when the input changes from high to low then capacitance on output is discharged through transistors. Power consumption is directly proportional to switching frequency. Switching at high frequencies leads to overall power consumption due to increase in threshold voltage of oxide layers of MOSFET.
- Dynamic power consumption: transient power consumption in addition with capacitive load power consumption together called as the dynamic power consumption. Transient means current flow in transistor switching from one logic level to another. Capacitive means additional power that is consumed in charging external load capacitance which depends on switching frequency.

If the capacitance is low, then the frequency of switching is high and transistor switching is faster. At the same time because of low capacitance power handling ability of transistor is greatly reduced.

(5) Register file size

This has great impact on power consumption. The register file size is the required number of register file involved in program execution. As the memory accommodating this register file goes on increasing, then the power consumed by the memory also is more. If the program execution time prolongs due to the processing of data from external devices execution time exceeds and energy consumed becomes more.

4. Various Techniques to Reduce Power Consumption

Embedded memories and logic libraries offer flexibility in selecting different design and power saving techniques. Power consumption has more to do with the CPU Architecture, transistor size and clock speed as discussed earlier. The most efficient is the architecture the more power is saved. more transistors are put in a small area reduces the amount of space between the transistor reducing the resistance producing less heat and allow to calculate more instructions per cycles. So each time new chip is made with more transistors it has new work to be done consuming low power and emerging as reliable as possible. Designing of a processor at 5 different levels such as circuit, system, architectural, gate and technology leads to low power consumption devices.

(1) System Level

System level design suggests that the inactive modules can be turned off to save the power. Most commonly used power reduction techniques are "SCALING". Scaling often requires (1) device technology (threshold voltage is lowered), (2) circuit design with lowering the transistor, (3) microarchitecture. Lowering the voltage ids not advantageous in contrast to it, a good low power micro architecture design can provide energy efficiency. Further efficiency can be achieved by avoiding the switching activities in idle units. These idle units power wastage can be reduced by clock gating at gate level. There are two types of scaling:

- Voltage scaling: voltage scaling means reducing the supply voltage and clock frequencies based on the work load. Benefit of voltage scaling is that it is much valuable for battery powered devices. Reducing the supply voltage is referred to be UNDERVOLTING that is most commonly used in real time applications such as laptops, mobile phones etc, there are 4 approaches to voltage scaling.

Static voltage scaling, multi level voltage scaling, dynamic voltage and frequency scaling, adaptive voltage scaling.

- Frequency scaling: this is also referred to be "CPU throttling". Is a technique where frequency of the processor is adjusted "on the fly" The dynamic power dissipated per unit time in noted and it accounts for two third of power consumption. the dynamic power is given by,

P(DYN)=C(EFF)*V^2(dd)*f

Where, C is capacitance f is frequency and Vdd is the voltage having greatest effect on power.

Scaling techniques are also used for reducing the heat in insufficiently cooled systems also. These are the some techniques at system level.

(2) Architectural Level

At architectural level, mainly capacitance is lowered and also the static and dynamic power consumptions that have been discussed earlier are also lowered. Static power consumption is due to the factors such as short circuit current, bias current, leakage current etc... In this level of design parallel hardware are used by means of two concepts known as the parallelism and pipelining. With these concepts the supply voltage of the processor is decreased and performance is increased by software techniques such as prediction and speculation (scaling), procedural lining, assembly in line, lop termination and thus parallelism is enhanced. Also we have Deterministic clock gating and pipeline branching as the techniques at the architectural level.

(3) Technological Level

Modern ICs operated with varying clock frequency and operating voltage has proved to work with longer battery life. Thus varying the voltage and the frequency has relationship with the delay and power consumption. At technology level design, we have to implement the following parameters in processors of embedded systems:

- Integrated hardware DMA and event system to offload the CPU in active and standby modes.
- Switching off or reducing clock or supply on device portions not in use.
- Intelligent sleep walking peripherals enabling CPU to remain in deep sleep.
- Fast wake up from low power modes and low voltage operation with full functionality.
- MCU design balancing of high performance /low leakage transition.

These factors can be implemented by means of pico power technologies. The low power features of embedded processor are multiple operating modes, automatic voltage regulator switching, automatic low power SRAM, low power battery backup modes. In order to achieve faster back up, digital frequency locked loops are preferred than the available phase locked loops. DFPL also eliminates the external component that reduces the total power consumption of embedded processor.

(4) Logic and Circuit Level

Power dissipation can be minimized by reducing the voltage using and also reducing the effective load capacitance. Here glitches occur due to the variation in signal arrival time. These glitches can be reduced by logic restructuring and path delay balancing techniques. These will reduce the power consumption at logic level greater. Use of hybrid library that uses CMOS circuit, pass transistor, equivalent pin can be done to reduce the power consumption. Minimization of the clock power can be done by: low swing clocking, clock distribution and clock gating which in turn saves energy.

5. Conclusion

Embedded system is more than part of human life. With a lot of functionalities being added, the need for high performance in embedded systems has become inevitable and so developers are increasingly leaning towards multicore processors in their systems designs decision. while this range of new applications also demand low thermal dissipation, low power consumption, real- time responsiveness, small physical form/footprint, low radiation/emission, hence reduction of power consumption techniques are essentially

needed. This paper gives an study on factors causing power consumption and reduction techniques that will be applied in real world usage and future applications.

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