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Study of static noise margin of SRAM based on supply voltage and topologies

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Abstract
This paper deals with the study of dependence of Static Noise Margin of SRAM on supply voltage and circuit topologies. Computation of Static Noise Margin of conventional 6T SRAM cell using butterfly curve and its corresponding read & writes operation where explained. This paper also investigates the effects of supply voltage, temperature & sizing of the transistors on SRAM performance. The results of SNM for various topologies and modifications in topologies for improving the performance in the subthreshold region and increasing the speed of the SRAM cell were discussed.

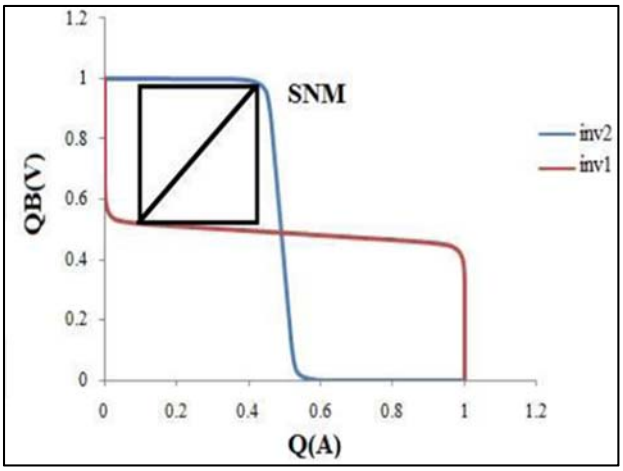
Keywords: SNM, Vdd, cell ratio, pull up ratio, Topology, stability

Introduction
Static Random Access Memory is a type of semiconductor memory that uses a bistable circuitry (flip-flop) to store each bit. The data can be retained as long as a sufficient power supply voltage is provided. SRAM is considered to be a critical component in a wide range of microelectronics applications [1]. There are three different modes of operation of SRAM they are standby mode, read mode & write mode. The improvement in performance of SRAM is achieved through the transistor scaling. As High supply voltage introduces a high leakage current, the supply voltage is lowered. This in turn decreases the threshold voltage. Reduction in the supply voltage also results in the reduction of static noise margin (SNM) & the performance of the device. The static noise margin of the SRAM cell depends on various factors such as cell ratio (CR), supply voltage, pull up ratio.
SRAM operates in the sub-threshold region when supply voltage is reduced. It reduces both the leakage power & access energy. During the operation when the SRAM cell is holding a data, its word-line is low, therefore the NMOS transistors are off. So, for proper holding of data, the back-to-back inverters in the SRAM cell must maintain a bistable operating points. This measure can be done effectively with the help of bit cell's SNM, which is the maximum amount of noise voltage that is introduced at the output of two inverters, so that the cell can retain its data. The plots between the voltage transfer characteristics (VTC) from inverter1 & inverse voltage transfer characteristics are used to determine the SNM. A two lobed curve is obtained called as the butterfly curve. Therefore SNM can be calculated as below,

SNM=Maximum side of the square
Maximum side of the square=maximum length of the diagonal/√2

Hence, SNM=maximum length of the diagonal/√2. It is assumed that a value Vn of noise source is to be introduced at the internal nodes of the bit cell. When Vn value increases from 0, inverse transfer characteristics of inv1 moves downward & VTC for second inverter moves to the right resulting in a curve meeting at two points. Similarly, for different values of the noise source, there is a change of SNM.

SRAM Modes of Operation
- Standby or hold mode
- Read mode
- Write mode



Butterfly curve of SNM

Standby mode

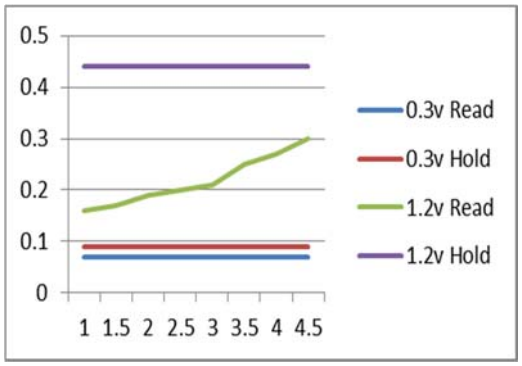
In this mode, the word-line is connected to ground. The cross-coupled inverter must be at bi-stable operating points to hold the data properly; this is achieved by means of SNM. The SNM equals the noise voltage necessary to flip the state.

Read mode

Here, the word-line is connected to Vdd, while the bit-line pairs are pre-charged to Vdd. As the voltage at the data storage node rises above the ground, the gain of the static transfer characteristic is lowered. This degrades the cell immunity to noise, as the cell is more sensitive.

Read margin characterizes the SRAM cell's read stability. Read margin is directly proportional to the cell ratio.

Cell ratio-Cell ratio can be defined as the ratio between the sizes of driver transistor to the load transistor during the read operation. If the cell ratio is increased, the current gets increased, which correspondingly increases the speed of the SRAM cell. It is given by, *CR= (W1/L1)/(W5/L5).* The plot among SNM Vs cell ratio is given below:



Write mode

In the write mode, it is assumed that the inverter-1 holds a data '0'&inverter-2 holds a data '1'.The word line is connected to Vdd, bit-line pairs are driven to Vdd & ground. Write Margin is defined as the minimum bit-line voltage required to flip the state of an SRAM cell. Write margin is directly proportional to the pull-up ratio. Write margin increases with the increased value of the pull-up ratio.

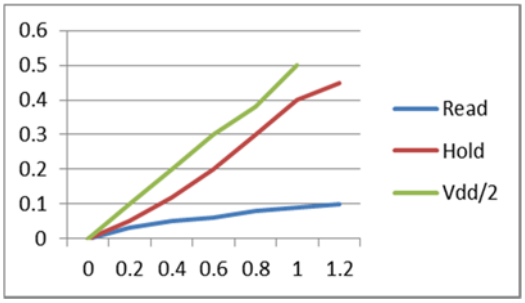
Pull up ratio- Pull up ratio can be defined as the ratio between sizes of the load transistor to the access transistor during the write operation. It can be expressed as, *PR=(W4/L4)/(W6/L6).*

Factors affecting SNM

The various factors that influence the static noise margin (SNM) are supply voltage, temperature & sizing of the transistors.

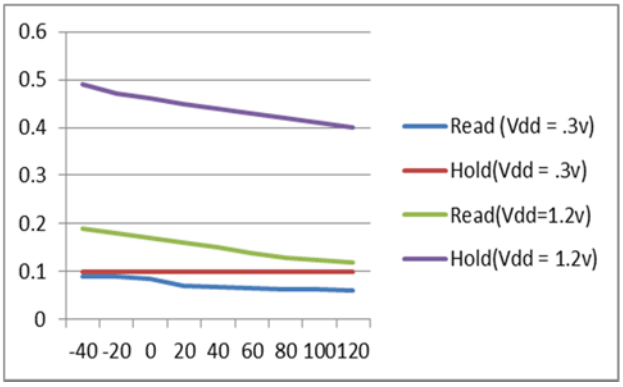
Effects of supply voltage (Vdd) on SNM

For retaining the bistability, only a minimum voltage is required. But the degraded SNM can limit the voltage scaling for SRAM designs above the required minimum voltage. It is observed that the SNM for a bit cell with ideal voltage transfer characteristics is limited to Vdd/2. The graph shown below gives a plot of SNM Vs Vdd for the hold & read modes.



Effects of Temperature on SNM

In subthreshold region, temperature variation has minimal effect on SNM. The reduction in SNM during standby with temperature is very small in comparison with reduction during read mode. In order to maintain stability temperature is normally kept between 25 C and 50 C. The plot shows temperature dependence of SNM in the sub-threshold operation.



Effects of transistor sizing on SNM

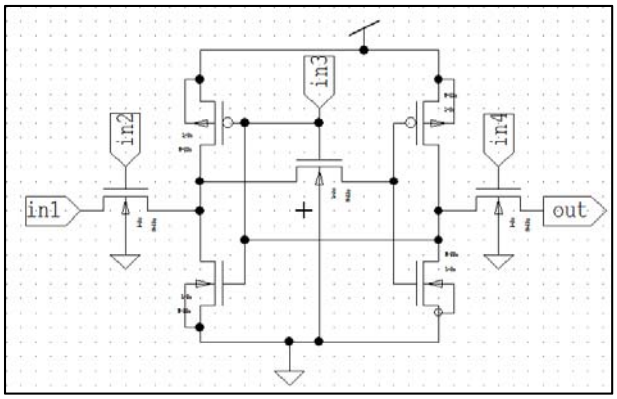
There is only a lower impact on sizing & have a logarithmic changes on the voltage transfer characteristics.

Various topologies of SRAM

This section deals with the analysis of various SRAM topologies working at different technologies, their implementation & the corresponding stability factor.

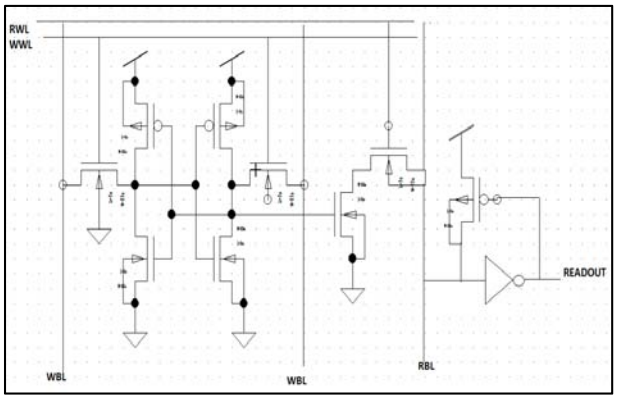
7T SRAM cell

A read SNM free SRAM at a lower Vdd, the write operation cannot be performed, & the read operation results in a severe destruction in the storage of data due to the leakage of PMOS cells. Whereas the other 7T SRAM cell uses a novel mechanism that uses only 2-bitline pairs to perform the write operation. Therefore, the write power saving is 49%. Thus the 7T SRAM cell has an improved SNM, & a good power saving operating at 720mv. There is 21% less leakage than conventional 6T.



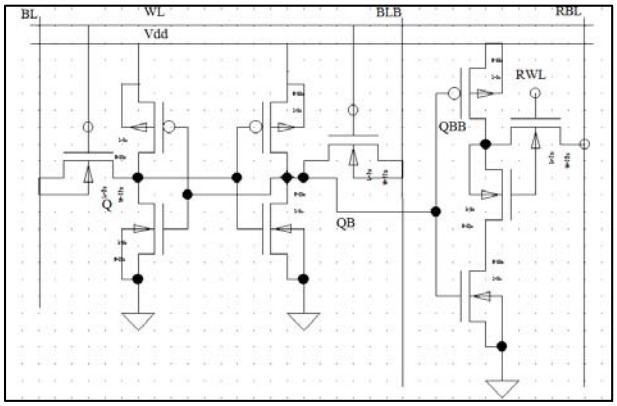
8T Sram Cell

The addition of two data output transistors to a conventional 6T –SRAM cell gives a 8TSRAM cell. As there is no cell degradation, the read SNM value is about 1.22 in contrary to the 6T-SRAM cell having a read value of 0.20.The contact area of WWL, word-line for write operations,& the two added transistors gives a 30% area overhead when compared to a conventional 6T-SRAM cell. However, there is an increased read stability & the power is constrained. The leakage reduction operates between 1.2V to 0.41V, but the design complexity increases.



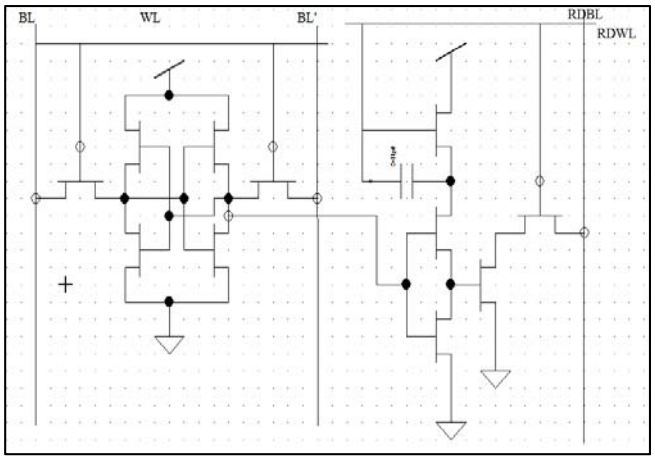
10T Sram Cell

In this type, either read or writes can occur per cycle & makes the SRAM work in the sub-threshold region. The problem of read SNM can be avoided by storing the read value in a buffer. The other types of 10T SRAM cell uses differential read bit-lines (RBL and \RBL).It comprises of two NMOS transistors for RBL and other additional NMOS transistors for /RBL. Therefore, there is an improved SNM & similarly WM is also improved. There is a 16% less leakage compared to conventional 6T.The only limitation is that, it has an inefficient area.



11T SRAM cell

The circuit comprises of two downsized transistors& a boost added to a conventional 6T SRAM cell. During the hold access the RDWL & WL are not selected, as the memory can have distinct read & write ports. The supply voltage is kept above 0.3V, so that there is a reliable speed provided with a proper write noise margin. The SNM is about more than 6 times compared with a conventional SRAM cell. Also there is a less power consumption, as it operates between 0.2V-0.35V and the area overhead is about 22-28%.



Conclusion

In this paper, we have analyzed about the static noise margin, read margin and write margin of a SRAM. It is observed that both the read margin & write margin depends on the cell ratio and the pull up ratio. The factors affecting SNM such as voltage, temperature and sizing of the transistors have also been studied. This paper tries to find out an efficient SRAM cell with high speed & performance.

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