International Journal of Applied Research

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Study of copper electroplating process for improved rf passive

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Abstract
In this paper portrays a thick copper plating measure dependent on silicon micromachining procedures, for manufacture of high-perspective proportion latent gadgets for high recurrence applications. Application to twisting inductors is hypothetically explored utilizing the concentric-ring model.

Keywords: Parental attitude, participation, sports, girls

1. Introduction
High region utilization and restricted execution are two of the primary downsides of aloof components coordinated in a radio-recurrence (RF) incorporated circuit measure. The restricted RF execution of planar, on-chip passives is brought about by misfortunes in the conveyor, just as in the leading silicon (Si) substrate, Conductor misfortune can be diminished by utilizing thick metallization layers, the overall pattern being the utilization of electroplated copper (Cu) as the top metal layer [1]. Nonetheless, this methodology is of restricted viability at high frequencies, because of the progression of current near the outside of the conductor (skin impact). An option is to utilize wide metal lines for the planar detached gadget. This, in any case, improves the capacitive coupling with the leading silicon substrate, fundamentally expanding the substrate RF misfortune. In spite of the fact that the last can be successfully stifled by utilizing high resistivity Si (HRS) substrates [2], utilizing wide metal lines isn't generally appealing because of an expansion in the general size of the gadget.

In this paper we propose a high-perspective proportion (HAR) copper electroplating measure as a way to diminish channel misfortune, while keeping the gadget region little. The gadgets are fabricated utilizing metal lines whose stature surpasses by a few times their width. An enormous bit of the current would then be able to stream along the vertical edges of the channels, decreasing the ohmic misfortune in the metal. In the interim, the width of the lines is kept little to limit the capacitive substrate coupling, and to decrease the general gadget zone. We will explore the adequacy of this methodology by hypothetically researching the quality factor of HAR winding inductors on both low-and high-resistivity silicon substrates in segment II. The cycle stream for manufacturing the planned structures, and creation subtleties are given in area III.

Simulation and Design
In order to study the effectiveness of the HAR process in improving the characteristics of spiral inductors we have considered four different technologies, depending on the metal and substrate used (Table 1). Note that the first process is the standard one based on 311m of Al on a low-resistivity Si (LRS) substrate. We next selected several (fixed) values of inductance, and calculated the inductor layout yielding the highest quality factor for each technology. The simulations were carried out for circular spiral inductors employing the concentric-ring model, with the layout of each coil defined in terms of its number of turns (N), radius (R), line width (w) and spacing (s).

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Table 1: Resistivities of the substrates and thicknesses of the metals are given in the table for different technologies considered in the optimization of inductors

Technology	Substrate	Metallization
A	LRS, 5Ωcm	3μ Al
B	LRS, 5Ωcm	15μ Cu
C	HRS, 2Ωcm	3μ Al
D	HRS, 2Ωcm	15μ Cu

Table 2: Optimum Q factor at 8 GHz for a 1 nH inductor with outer radius of 120 urn. N is # of turns, W is the conductor line width, and S is spacing between the windings.

Technology	Layout	Q (8GHz)
A	N=2, W=6.5μm, S=28.9μm	13.8
B	N=2, W=5.0μm, S=22.4μm	23.6
C	N=2, W=16.4μm, S=7.6μm	25.3
D	N=2, W=11.4μm, S=9.3μm	48.6

For instance, Table 2 shows the registered design of ideal 1 - nH inductors at 8 GHz for a fixed span of R=120 urn. The ideal number of turns, line-width dividing are diverse for various advancements as can be seen from Table 2. Figure 1 shows the inductance (L) and quality factor (Q) of each loop as capacity of recurrence. On both low-and high-resistivity substrates, the utilization of HAR method prompts an enormous expansion in Q, as can be seen from Fig. I. This expansion is more huge for the loops on high-resistivity Si, where it is kept up until high frequencies. On the low resistivity substrate the pinnacle of the Q bend happens significantly sooner, restricting the most extreme recurrence of the inductors.
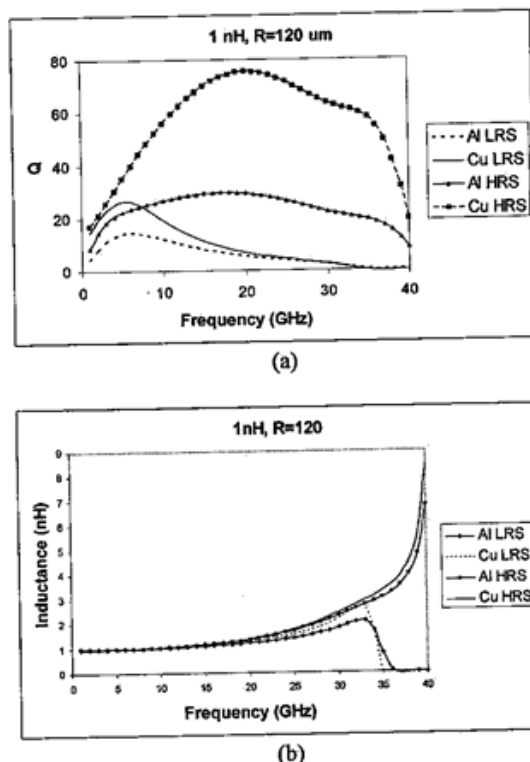

Fig 1: (a) Q and (b) L results for four different optimized cases. Inductance is lnH at 8 GHz which is the optimization frequency
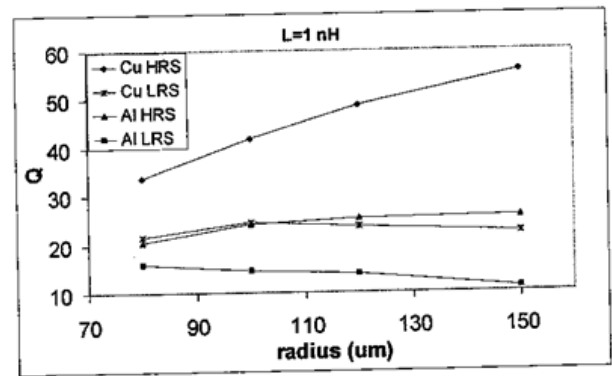

Fig 2: Q factor as function of radius (R) for a I nil inductor at 8 GHz

Table 3: Optimum Q factor at 0.8 GHz for a 10 nH inductor with outer radius of 300 urn. N is # of turns, W is the conductor line width, and S is spacing between the windings

Technology	Layout	Q (8GHz)
A	N=4, W=23.45μm, S=10.86μm	13.8
B	N=4, W=10.04μm, S=24.34μm	23.6
C	N=4, W=26.24μm, S=4.07μm	25.3
D	N=4, W=13.61μm, S=17.78μm	48.6

It is imperative to tolerate at the top of the priority list that the ideal estimation of Q relies upon the size (sweep) of the inductor. In figure 2 we have demonstrated the most extreme Q got for every innovation, as capacity of the inductor sweep R. Note that the most extreme feasible Q on high-resistivity substrates increments with expanding inductor size. This is on the grounds that on those substrates, expanding the inductor region permits one to oblige more extensive lines, subsequently lessening the conductor misfortune. On low-resistivity Si, be that as it may, a bigger territory infers a bigger capacitance to the substrate and, along these lines, expanded substrate misfortune. Thus, the ideal Q doesn't monotonically increment with expanding size on low-resistivity substrates (Fig 2).

Table 3: Optimum Q factor at 0.8 GHz for a 10 nH inductor with outer radius of 300 urn. N is # of turns, W is the conductor line width, and S is spacing between the windings.

Technology	Layout	Q (8GHz)
A	N=4, W=23.45μm, S=10.86μm	13.8
B	N=4, W=10.04μm, S=24.34μm	23.6
C	N=4, W=26.24μm, S=4.07μm	25.3
D	N=4, W=13.61μm, S=17.78μm	48.6

As another model we have streamlined 10nH inductors with a span of 300μm at 0.8 GHz for every innovation in table 3. The L and Q of the inductors are plotted in Fig 3 as capacity of recurrence. Concerning the lnH inductors, the utilization of HAR copper again prompts a higher Q esteem by and large. Note that in the event of the high-resistivity substrate, the general improvement noticed is more modest than that of the lnH loop. This might be credited to the bigger number of turns and, henceforth, expanded current swarming impact in the curls.
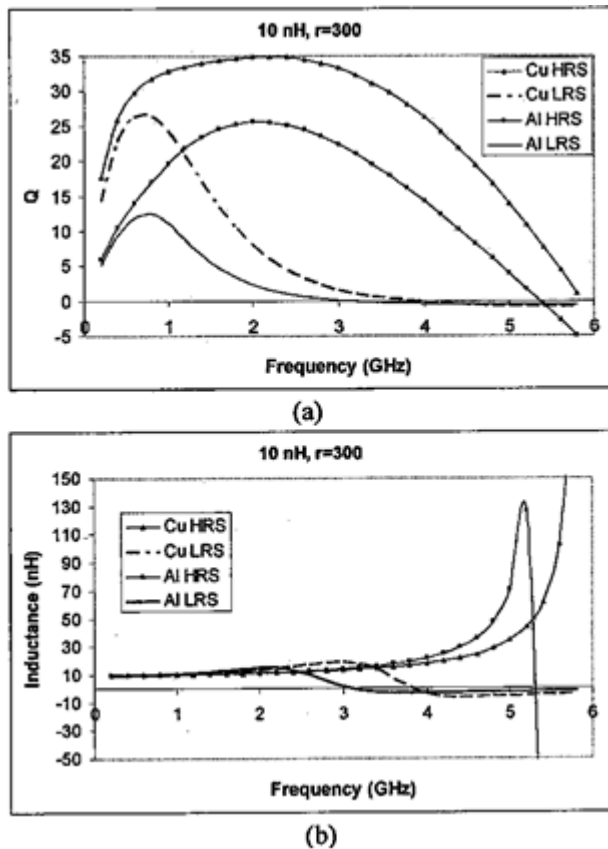
(a)

(b)

Fig 3: (a) Q (b) L results for 10 nH inductors optimized at 0.8 GHz

Fabrication

Manufacture of the thick copper inductors is a savvy single veil step measure, which is intended to be a post cycle module for completed RF IC wafers. Cycle stream, which is additionally given in Figure 4, begins with the faltering of the seed layer, for this situation Ti/TiN/Cu. Ti is utilized as a bond layer and TiN is utilized as a dispersion hindrance for copper. Copper is the real seed layer, which goes about as a conduction cushion for current during electroplating. The thickness of Ti layer is 10 nm, which is adequate for bond. The thickness of the TiN and Cu layers is 40nm and 300nm, individually. The Cu layer should be thick enough to make low protection from forestall any nonuniformity in likely dispersion during copper electroplating.

The second step involves the formation of a mold using thick photoresist. Photoresist can be easily patterned using lithography and can be removed by acetone. These are the two advantages which make thick photoresist more attractive than polyimides or Sur for such a process [3]. The photoresist used in the process is AZ 4562. It is spin coated at 800 rpm to give sufficient thickness (~l8 urn) for electroplating. One of the important steps in the process is the baking of the photoresist. Since it is a very thick layer, baking time significantly increases. The surface of the photoresist dries during baking and forms a hard surface. This surface prevents the solvents below to evaporate, which is the main cause of longer baking time. If baking is not done properly, unexposed photoresist is also developed in the developer, which leads to a poor pattern resolution.

All of the process steps are performed at temperatures lower than 150 °C. Therefore, they are thermally compatible with the RF-IC processing. Also copper diffusion is prevented by the TiN layer, which makes the process compatible in terms of contamination control, it can also be considered as a cost effective post process since there is only one lithography step.

Conclusion

High-viewpoint proportion copper plating measure essentially improves the quality factor of coordinated twisting inductors on both low-and high-resistivity Si substrates by diminishing the curl opposition. Manufacture is accomplished by a basic savvy measure viable with RF-IC innovation and can be utilized as a post cycle module for improved uninvolved part execution.

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